THE UNIVERSITY OF CHICAGO

THE USE OF BLOCK-COPOLYMER NANOLITHOGRAPHY TO FABRICATE ULTRAFINE PHONONIC CRYSTALS AND PHONONIC CRYSTAL-ENHANCED DEVICES

A DISSERTATION SUBMITTED TO

THE FACULTY OF THE PRITZKER SCHOOL OF MOLECULAR ENGINEERING

IN CANDIDACY FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

BY

ELIZABETH MICHIKO ASHLEY

CHICAGO, ILLINOIS

MARCH 2021

DEDICATION

To Michiko Iwata Hansen, who introduced me to the beauty of crystals (and rocks). This dissertation would not exist without you.

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Acknowledgements

It is a very surreal feeling to be sitting at my desk writing the acknowledgements for this dissertation during a global pandemic that has forced us into extreme social isolation and destroyed life as we knew it. I just wanted to, on the record, comment on the unusual circumstances under which I finally completed this 6-year dissertation so that I never forget.

Pandemics aside – my journey to this point has been pretty nonlinear, and I would literally not be here right now without a number of very important and influential people in my life. I want to thank my parents, Clint and Teresa Ashley, for raising me and supporting me unconditionally, for prioritizing my education from an early age, for encouraging my creativity and curiosity, and for introducing me to STEM. In particular, I want to thank my mother for always being there for me when I called her to complain about my research or when I thought I couldn't go on. If she charged me hourly I'm sure she'd be a multi-millionaire by now.

I also would like to thank my siblings, Catherine and Noah, who have become important daily fixtures in my life. Our family is small, but knowing that there are two people who truly understand me made it possible for me to survive research. Spending time with them virtually during the pandemic while I was writing my thesis alone in my apartment for months at a time was probably the single most critical sanity booster for me. They are my B+ squad forever.

I'd like to thank my undergrad advisors at UMD, Dr. Robert Briber and Dr. Ichiro Takeuchi for taking a chance on me as an undergrad and introducing me to laboratory research. I'd also like to thank my internship advisors at NIST, Joe Kline and Dan Sunday, for patiently introducing me to block-copolymers, synchrotron radiation, and MATLAB. Joe and Dan pointed me towards the Nealey group at UChicago when I mentioned I was applying for grad school, and I wouldn't have ended up doing research at UChicago without their mentorship and guidance.

I owe a special thanks to my advisor, Paul Nealey, for giving me a chance in his group and never giving up on me, despite the rather large learning curve I was up against. Under his guidance, I was able to grow from a confused first year to a (somewhat) competent fabrication scientist, and I am incredibly grateful for the opportunity I was extended and patient support I received. I'd also like to thank my collaborators Kouhei, Naoki, and Masaki from Panasonic, Japan – this work couldn't have happened without them. I also owe a special shout-out to the PNF technical director Peter Duda, who not only tolerated my sense of humour, but also encouraged it. I could not have completed my thesis experiments without him. I will always fondly remember our musical trio, The Phonons, and the PNF celebrations that we headlined with the support of Joel, Sally, and Mike.

Next up are my friends and colleagues from grad school. Moshe deserves a special mention. He was always there to grab a Div School coffee and a fried chicken sandwich and to mine the internet for savage memes with me. He was both my biggest source of support in the Nealey group and one of my closest friends at UChicago. I have a lot of other friends and colleagues who helped keep me sane throughout this degree, including Anna, Arin, Taylor, Jeronimo, Joel, Joe, Joe, and Claire, to name just a few. I'd like to broadly thank everyone else who helped me get by, including my research group, my various collaborators, my a cappella group, and the other PNF superusers.

Next, I would like to thank my closest friends who have supported me over the years (and through the pandemic especially), starting with my best friends from UMD, Mark and Nick. Mark has been like a brother to me over the years, and Nick has shared my pain as a phonon-oriented PhD student. I owe special thanks to Linsin for being one of my closest and most supportive friends at UChicago, especially during this final stretch of writing, and getting through the end of 2020 into 2021 would have been miserable without her. I'd like to extend an extra-special thanks

to my favourite Canadian, Jon. I will always fondly remember the special adventures and rock times we shared during my time in grad school.

Finally, I must thank my grandmother, Michiko, who unfortunately is no longer here with us. She influenced my life in immeasurable ways. I admired her so much for her strength, intelligence, and resilience, and am forever indebted to her for enabling me to get a college education. I think she would be pleased to see some return on her investment.

As a final note, I wanted to document that while I very much wanted to title this dissertation "Advanced Hole Punching II", I ultimately refrained from doing so.

Abstract

In recent years, phononic crystals have emerged as a possible route for engineering the thermal properties of semiconductor materials like silicon independently of their electronic properties. Heat carriers, or thermal phonons, in Si are very difficult to manipulate due to their wide range of frequencies and nanoscale size. Nanostructures are required to most effectively manipulate thermal phonons, but are extremely difficult to fabricate due to resolution limitations of modern lithography equipment. We present in this work several different block-copolymer nanolithography-based approaches for fabricating sub-resolution limit hexagonal arrays of holes at a pitch of 37.5 nm with an overall porosity of ~42% in Si materials that functioned as phononic crystals. In addition to fabrication details, thermal conductivity measurements are presented for several Si-based phononic crystals and a prototypical phononic crystal-enhanced IR sensor. The overall theme of this work was to expand the experimental understanding of low-dimensional thermal phonon transport in nanostructured materials, with an emphasis on probing the roles of incoherent and coherent scattering, and diffusive and ballistic transport under ambient conditions. We demonstrate that Si nanostructures templated by block-copolymer nanolithography effectively function as phononic crystals capable of reducing the thermal conductivity by 80-90% relative to bulk. We also demonstrate that the orientation of nanostructures with respect to the direction of heat flow at these length scales has a measurable effect on the thermal conductivity.

Chapter 1: Introduction to block-copolymer directed self-assembly, nanolithography, phonons, and phononic crystal fabrication

1.1 Lithography and phononic crystals

The rapidly diminishing feature sizes in modern electronic devices has led to a technological revolution over the past several decades. As devices have shrunk to the single- and tens-of-nanometers scale, a number of engineering challenges have emerged, ranging from resolution limits of lithographic equipment to limits on materials selection for continuing to improve device performance. Lithographically, resolution limits are limited practically to ~30-80 nm, which rely heavily on complex and time- and resource-expensive self-aligned multiple patterning strategies based on 193i immersion lithography. The electronic and mechanical properties of materials with dimensions on the order of a few tens of nanometers are subject to performance degradation due to materials properties varying between the nanoscale and bulk. A primary source of performance degradation at the nanoscale is poor thermal management. The nature of thermal management required for optimal performance depends on the device- for cooling applications, larger thermal conductivity is desirable, while for IR sensors, low thermal conductivity supports are critical to the sensitivity of the device.

Currently, technologies such as thermoelectric generators and IR sensors are close to the materials selection limit; i.e., optimizing the electronic and thermal material properties for improved device performance is no longer a long-term viable design approach for continually enhanced devices. Furthermore, materials used in these applications (i.e. VO_x) tend to be rare, expensive, and challenging to incorporate into micromachining processes. Materials that have desirable electronic properties for these applications typically have undesirably large thermal conductivities that hamper performance. The ideal material for thermally sensitive applications

would have fully customizable thermal and electronic conductivity, which is challenging as both are material dependent intensive properties.

One emerging potential route for improving the design and efficiency of these devices is to manufacture them monolithically from silicon (Si). Si is a highly desirable material for electronic devices because its electronic properties can be fully customized by selective ion implantation. The disadvantage of Si is that it has a large native thermal conductivity. However, an innovative approach for reducing the thermal conductivity of Si has been introduced in recent literature: creating Si nanostructures with anomalously low thermal conductivity, called phononic crystals. Phononic crystals are periodic, elastically mismatched binary materials that typically consist of periodic voids created in some material like Si. Phononic crystals are thought to function predominantly by incoherently scattering phonons, the primary heat carrier in Si. How well a phononic crystal scatters phonons (i.e. how much a phononic nanostructure reduces the thermal conductivity of the host material) depends on the minimum dimension of the structure. Thermal phonons consist of THz frequency vibrations, and thus can only be effectively scattered by nanoscale structures.

While a number of phononic crystals have been fabricated and studied experimentally with minimum dimensions ranging from a few hundred nanometers to micrometers in scale, larger dimensions are not as effective phonon scatterers because the phonon wavelengths are very small (~ few nm) and the mean free paths of phonons in Si can be rather large- up to a micrometer. Manipulating phonons most effectively in nanostructured materials is also limited by the relative paucity of experimentally verified understanding of low-dimensional phonon transport, especially in nanostructured systems. This is due in part to the resolution limit of conventional lithographic processes, as fabricating structures with a few nanometers of periodicity is almost impossible to

do, especially in large volume. While several studies have produced phononic nanostructures with periodicities in the range of 30-50 nm, the structures have been low-volume with large variation sample-to-sample due to poorly controlled defectivity and roughness.

One potential route to address the resolution limitations and nanostructure quality problems is using block-copolymer directed self-assembly nanolithography to create porous nanostructures needed for phononic crystal research. BCPs tend to self-assemble into well-ordered nanostructures across large areas with isodimensional, thermodynamically determined features. BCP nanostructures can be oriented into defect-free perfect single-orientation regions by directed self-assembly at length scales unattainable conventional lithographic equipment in very few steps relative to self-aligned multiple processing strategies. Furthermore, BCP nanostructures are easily integrated with Si micromachining processes, allowing their nanostructures to be transferred into technologically useful materials like Si. These attributes make BCP nanolithography a highly lucrative potential route for fabricating high precision phononic crystals at the minute length scales required to sensitively probe low-dimensional phonon transport and to engineer the thermal conductivity of Si.

In this work, we present the development of fabrication processes implementing BCP nanolithography to fabricate ultra-low thermal conductivity devices from a silicon-based materials as part of an industrial collaboration with Panasonic. We first present introductory information on block-copolymers, nanolithography, and phononic crystals. Next, we describe the fabrication and measurement of phononic crystals in amorphous silicon nitride, where we studied nanoscale heat transport in structures ranging from 37.5 nm to 1600 nm. Next, we present the fabrication and measurement of a polysilicon IR sensor, which was enhanced by phononic crystal nanostructure templated by BCP nanolithography. We also present discussion regarding assessing BCP

suitability for nanolithographic pattern transfer, processing challenges for complex nanostructures, and a discussion of nanoscale etch rate differences that are important to consider when fabricating low dimensional structures. Finally, we present a combined experimental and simulation-based effort to fabricate, and measure, and interpret the performance of DSA-templated Si phononic crystals with varying nanostructure orientation with respect to the direction of heat flow.

Throughout this work, we were able to fabricate ultra-low dimensional Si nanostructures with pitches of 37.5 nm, hole radii of 12.5 nm, and porosities of 40-42%, which effectively reduced the thermal conductivities of our nanostructures 80-90% relative to bulk. We extended understanding of phonon transport from larger-scale experiments into the <20 nm regime and demonstrated that thermal conductivity reduction in nanoscale phononic crystals is largely governed by increased phonon scattering from boundaries in low dimensional structures. Furthermore, we demonstrated that the orientation of aligned channels with respect to the primary direction of heat flow through a nanostructure measurably affects the thermal conductivity. Overall, we meticulously expanded understanding of how thermal conductivity is reduced and how to design an effective phononic crystal into the <20 nm regime through a combination of experimental and simulated measurements on Si phononic crystal nanostructures with dimensions and precision previously unattainable in the literature.

1.2 Introduction to block-copolymers

Block-copolymers (BCPs) are a diverse class of soft materials that have been extensively studied for several decades due to their ability to spontaneously assemble into a wide variety of highly regular nanostructures. Broadly, BCPs are a class of polymers consisting of two or more different polymer blocks (a contiguous region of one chemistry) that are chemically attached to each other at the molecular level[1]. Due to the differing chemical properties of each distinct block,

BCPs tend to phase separate into a variety of periodic and complex nanostructures with very narrow distributions in feature size. There are a vast range of potential applications for BCPs including drug delivery, metamaterials, conductive polymers, micro- and nanofluidics, and ultra-fine sub-lithographic templating.

Many different types of BCPs have been studied in recent decades, including (but in no way limited to) linear (diblock, triblock, etc.) copolymers, starblock copolymers, and branched copolymers. Examples of these different chain architectures for two-block systems are shown in Figure 1.1. Each BCP has a unique phase diagram that is a function of its molecular weight and composition. A number of BCP phases have been reported, ranging from relatively simple phases like lamellae, spheres, and cylinders, to complex phases like bi- and tri-continuous gyroids[2–4], σ-phases[5,6], and quasicrystals. Some phases are so complex that they have earned humorous colloquial names, such as the distorted gyroidal phase fondly known as "plumber's nightmare."[7]

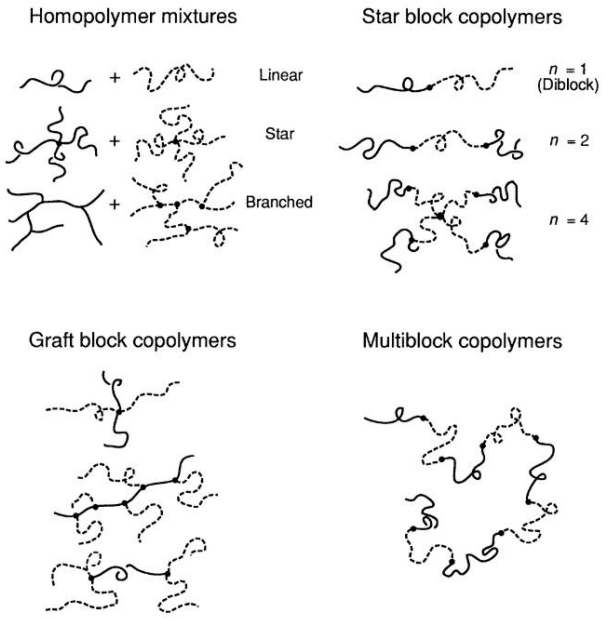

Figure 1.1 Examples of polymer-polymer molecular architectures that can be formed from polymerization of two different monomers. Figure taken from Science, Vol 251 (898-905), 1991[8].

BCPs tend to form highly ordered microdomains with dimensions that typically between 5-50 nm[9]. While BCPs microstructures have been studied both in thin films (~ >500 nm) and in bulk, in this work we will focus exclusively on thin-films (<100 nm). The standard approach to prepare a BCP thin film begins dissolution into an organic solvent, spin-coating the solution on top of a target substrate (typically a silicon wafer), and annealing at an elevated temperature achieve phase separation. The sizes and shapes of the microdomains are governed by the molecular weight, composition, chemical functionality of the blocks, and annealing temperature. Interfacial energy between the BCP and both the bottom and top interfaces significantly affects the final morphology of the film as well[10].

The microphase behavior of a BCP system is caused by the chemical bond that prevents the two phases (in the case of diblock copolymers) from macroscopically separating. As a result, BCPs microphase separate at a length scale comparable to the dimensions of the polymer molecule. The resulting microstructure exhibits very different phase behavior than is seen in macroscopic phase separation for conventional binary systems like oil and water mixtures[8]. Examples of different kinds of phases that have been reported for linear block copolymers are shown in Figure 1.2.

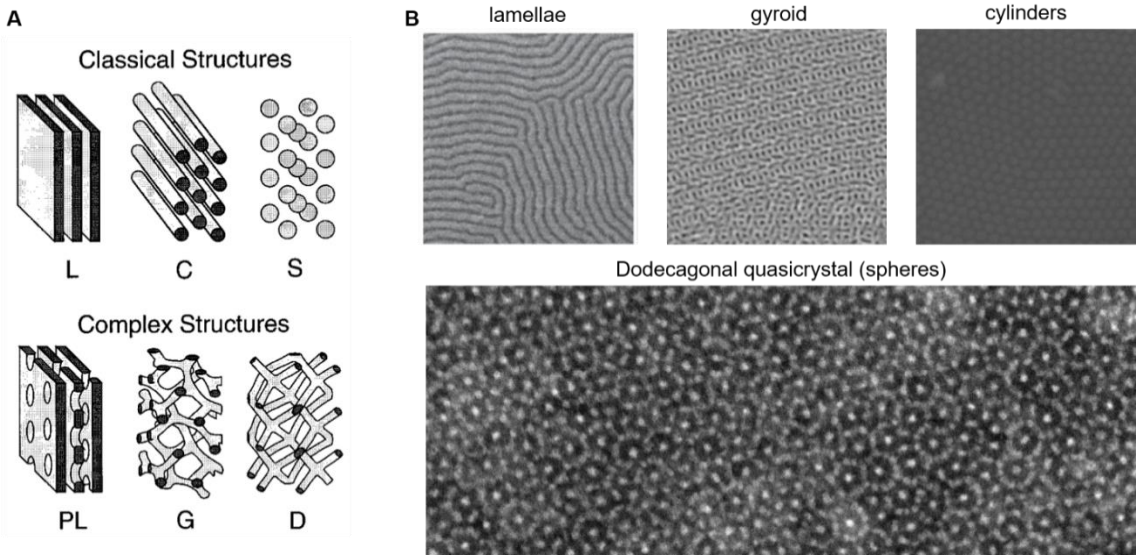

Figure 1.2 Examples of phases that have been reported in linear diblock copolymer systems. In (A), schematic illustrations of classic and complex structures formed in a linear diblock system are shown, taken from Phys. 106, 2436–2448 (1997).[11] In (B), SEM micrographs of lamellar[12], gyroidal[13], cylindrical, and quasicrystalline microstructures are shown. The images of lamellar and gyroidal phases were taken from the indicated references, while the images of cylindrical and quasicrystalline BCP phases are the author's own work (pending).

1.3 Linear diblock copolymers

The phase behavior of BCP systems, as mentioned previously, is generally dependent on the composition, molecular architecture, number of segments *N*, and monomer chemistry of the BCP system.[8,10,11] The equilibrium phases formed by a BCP are governed by complex thermodynamics, and constitute a delicate balance between enthalpic and entropic factors that are combined to form the Gibbs Equation of State,

$$G = H - TS. \tag{1.1}$$

where G is the Gibbs Free Energy, H is enthalpic contributions (H = UPV, where U is the system energy, P is the pressure, and V is the volume), and S is entropic contributions. Thermodynamic models to predict the phase behavior of BCPs are derived from G, and often result in representation of phase space as a two-dimensional function of the fraction of a given block and a variable derived from the Flory-Huggins parameter χ[8]. The composition of a linear diblock system is generally

represented by f for one block ($0 < f < 1$). Experimentally, for each new A:B composition ratio, a new BCP must be synthesized.

The Flory-Huggins parameter χ describes the energetic and entropic penalties that result from A-B segment-segment interactions, and (roughly) describes the degree to which the different blocks will phase separate. The strength of this separation strongly influences the phase behavior of a system, and is a function of the different block chemistries. χ is written as

$$\chi = \frac{1}{k_B T}\left[\epsilon_{AB} - \frac{1}{2}(\epsilon_{AA} + \epsilon_{BB})\right] \tag{1.2}$$

where k_B is the Boltzmann constant and ε_{ij} is the interfacial energy between segments i and j.[8] A positive value for χ_{AB} implies that the interfacial energy cost for A-B mixing is lower than the sum of interfacial energies for A-A and B-B interactions. In this circumstance, phase separation will not occur as mixing is energetically less expensive. However, a negative value of χ_{AB} implies that the energetic cost of A-B mixing is larger than the sum of the energetic costs of A-A and B-B mixing, meaning that phase separation is energetically favored over mixing. Thus, both the magnitude and sign of χ are important when describing the strength of phase separation for a given diblock system.

In addition to χ, the size of the chain, or number of segments N, is critical in determining the polymer phase behavior. In a melt, BCPs have a statistical length that is a function of the monomer chemistry and architecture and the stiffness of the chain. Stretching the chain beyond its equilibrium size incurs an entropic penalty upon mixing. However, A-B interactions also represent an energetic penalty. For a system that phase separates, the equilibrium morphology is a balance of entropic costs (stretching chains into ordered configurations) and the minimization of system interfacial energy (minimizing the total A-B interfacial area). As chain size increases with N, reorientation of chains into ordered configurations becomes increasingly slow and energy

expensive, making phase separation challenging for chains with large N (M_w > 80k). Thus, phase separation behavior of a system is better described by the parameter χN, which accounts for both the interfacial energies of the blocks and configurational challenges that scale with chain size.

An example of a phase diagram for a symmetric (blocks A and B have equivalent statistical lengths) linear diblock copolymer is shown in Figure 1.3. As χN increases above ~10.4, the polymer transitions from a disordered state to an ordered state with a phase determined by its composition. This point is called the order-disorder transition (ODT). As f increases, the polymer moves through several phases, primarily spherical, cylindrical, and lamellar phases. Some phases, such as lamellar and cylindrical phases, occupy large areas of phase space over a range of values of χN and f, and are thus relatively easily formed. Others, like the gyroidal phase, occupy very narrow regions of phase space and are thus difficult to obtain experimentally. The most technologically useful BCPs for integration into lithographic processes are lamellae and cylinders because each occupy a relatively large portion of phase space, are well studied, and are relatively easy to obtain, in addition to enabling formation of useful shapes in processes (i.e. lines, holes).

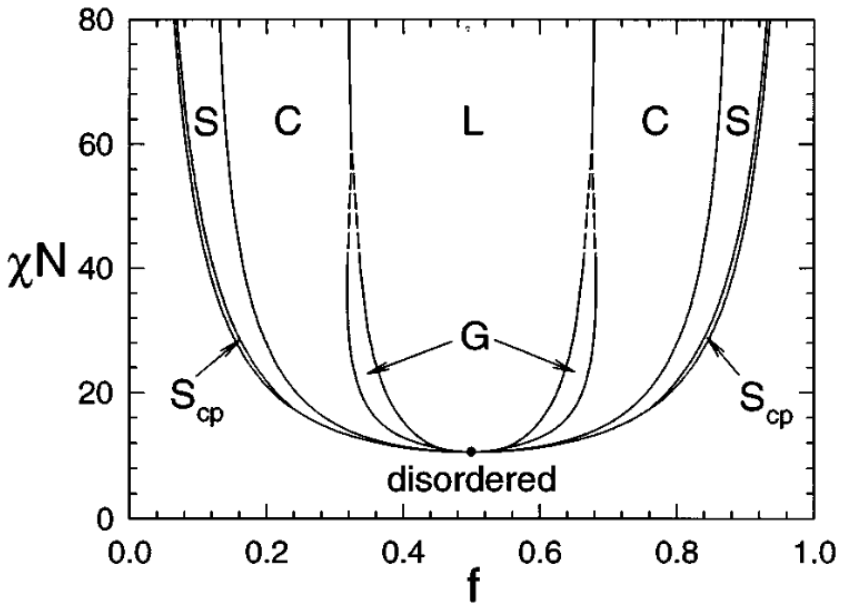

Figure 1.3 The mean-field phase diagram for a symmetric, linear diblock BCP melt calculated via self-consistent field theory (SCFT). The different phases formed in this system are labeled S_{cp} (close-packed spherical), S (spherical), C (cylindrical), L (lamellar), and G (gyroid). Figure taken from J. Chem. Phys., Vol. 106, No. 6, 8 February 1997.[11]

1.4 Modern nanolithography strategies

Over the past several decades, enormous progress has been made in electronic technology. Computers and related devices have become smaller, faster, and more efficient, with significantly larger memory, thanks to significant advances in lithographic techniques. These technological advancements have largely been driven by the need for increasingly smaller feature sizes for transistors in chip manufacturing. Moore's law is a concept that describes this phenomenon, stating that for technology to keep progressing at the same rate, the number of transistors on a chip must double every two years. Until approximately the mid-2000s, this "law" held true, and smaller feature sizes were regularly obtained via decreasing the wavelength of light used for lithographic patterning and other improvements.

In the modern era, the feature sizes of devices are comparable to the wavelength of the light used for patterning, which problematic because it is impossible write patterns smaller than

the wavelengths of light in a tool. Current industry standard relies on 193 nm immersion lithography (193i), which has reached its physical resolution limit[14]. Extreme ultraviolet (EUV) light with a wavelength of 13.5 nm has been ardently sought after since 2004, but industrial implementation has been hampered by a number of issues related to source power, high energy stochastics, and large expense[10,14–16].

A number of clever approaches to circumvent the resolution limits of conventional lithographic tools have been devised, including litho etch litho etch (LELE or LE^2) and self-aligned multiple patterning (SADP, SAQP, and SAOP for double-, quadruple-, and octuple patterning, respectively). Examples of these lithographic techniques are shown in Figure 4. In LELE, the substrate is patterned then etched at least two times, with the second lithographic pattern being offset by the desired xy spacing, to achieve sub-resolution lithography. While relatively simple in concept, this method suffers from overlay issues as dimensions approach 22 nm and smaller and requires costly extra processing[17]. Self-aligned multiple patterning (SAMP) is an attractive alternative to LELE. In SADP, a resist is exposed and developed, and a masking material is then deposited. This material is then etched to form sidewall spacers. Finally, the resist is removed, and the spacers are used as a mask to etch the underlying material.

While SAMP eliminates the overlay issues endemic to LELE and requires only one major exposure, it suffers from issues of pitch walking and is only suitable for regular patterns. One of the biggest issues with LELE, SAMP, and other multiple-patterning strategies is that they require multiple etch steps to achieve the nanostructure dimensions required for continually shrinking transistor feature sizes, in which fin pitches are currently around 34 nm for Intel's 10nm node[18]. This is both expensive and time consuming, and subject to overlay and roughness issues as the number of process steps increases. Electron-beam lithography (EBL), while capable of patterning

with in-plane resolution of a few tens of nm, is a serial technique and is extremely slow and expensive by comparison, and does not have the throughput required to be implemented at an industrial scale, among other issues[10].

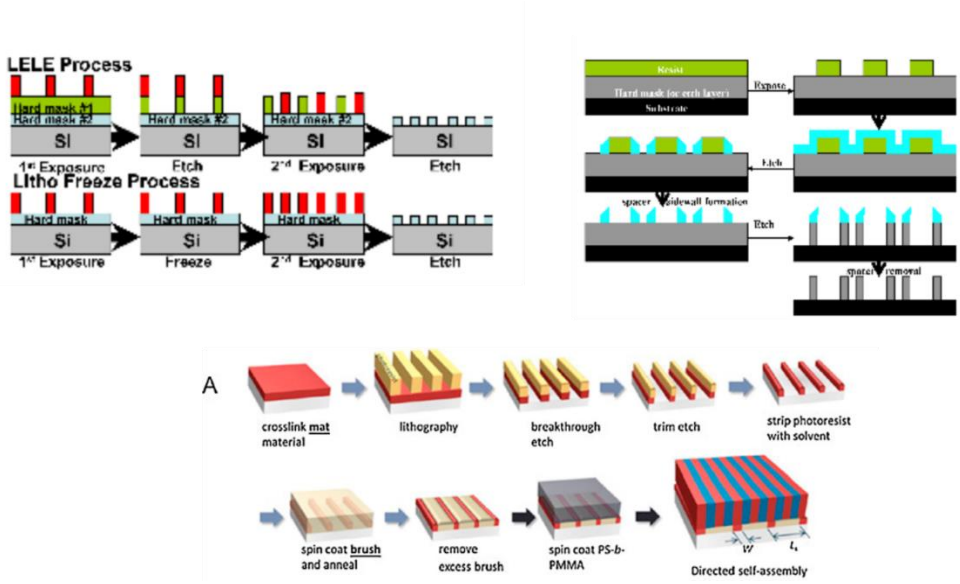

Figure 1.4 Illustration of various lithographic patterning strategies designed to achieve sub-lithographic patterning. At the top, LELE approach is shown on the left, while SADP is shown on the right[17]. Below, an example of a DSA process flow for generating nanoscopic lines is shown. Note the process simplicity relative to LELE and SADP[10]. Figures taken from P. Zimmerman, *SPIE Newsroom* (2009) and *Prog. Polym. Sci*. **54**–**55**, 76–127 (2016).

Directed self-assembly (DSA) of BCPs has emerged as a highly attractive alternative to multiple patterning processes due to its ability to form highly regular, self-assembled features in a single etch step. Natively, BCPs phase separate and form highly ordered microstructures that are polycrystalline, consisting of grains of a single-orientation separated from neighboring grains by complex biphasic defect structures. Defects are not acceptable features in most circumstances because nanostructured devices require extremely narrow and controllable feature sizes. To solve this problem, DSA was developed by the Nealey group in the mid-2000s[19].

To achieve DSA, a chemical template capable of guiding the assembly of a BCP melt into a single-orientation region is fabricated. An example of a DSA process to form lines is shown in

the bottom of Figure 1.4. Generally in a chemoepitaxial DSA process, the first step is to deposit a polymer film that is energetically neutral to both blocks. Then, a resist is deposited on top of this film and patterned, in the case of a lamellar BCP, with lines spaced at some multiple of the native pitch of the polymer, L_0. Then, a polymer preferential to one of the blocks is grafted to the lines etched in the previous step to complete the formation of a chemical template. Finally, the BCP film is coated and annealed. Due to the presence of the chemical template, it becomes energetically favorable for the BCP to assemble into a single-orientation region over the template, resulting in perfect assembly. After this step, the BCP can be used as an etch template to transfer its structure into some underlying material (often, silicon).

The world of DSA is very diverse. A variety of diblock copolymers, phases, pattern transfer methods, and end applications have been extensively researched both for industrial and academic purposes. DSA is currently the only self-assembly technique capable of producing sub-lithographic features over large (user-defined) areas, and has the advantage of being compatible with existing processes. Furthermore, the chemical templates needed to guide the BCP assembly can be fabricated on conventional lithography equipment (193i, EBL), allowing the potential "increase" of the resolution limits of these tools.

While DSA continues to suffer from defect densities that make it challenging to incorporate into mass produced industrial lines, computational and experimental research partnerships have made extensive progress in the last few decades in understanding defect formation and annihilation pathways. DSA still has enormous potential to shrink the feature sizes and improve feature quality in nanolithographic processes[10,15,20]. For device research applications that require nanoscopic feature sizes in which industrial-scale defect densities are not an important consideration, the potential uses for DSA are even more diverse.

1.5 Directed self-assembly

In order to direct the self-assembly of a BCP, the polymer must first be induced to assemble in a perpendicular orientation. For this to occur, both blocks of the polymer must be able to wet the surface. Equal surface wetting will only occur when the blocks have roughly equivalent interfacial energy at both the top and bottom interface[21,22]. If either the top or bottom interface has a lower interfacial energy with one block, that block will preferentially wet the interface, resulting in parallel morphology. Perpendicular assembly is required for a BCP to be useful for etch-transfer. Dry (plasma) etching, which is a top-down anisotropic process, is typically used for etch transfer. Phases like lamellae and cylinders are thus far more useful than sphere phases because they form continuous domains in the vertical direction, and can thus be relatively easily pattern-transferred with high precision and etch contrast.

In addition to the phase type, the surface free energy (SFE) of a copolymer system is important in determining its ease of incorporation into a process. Poly(styrene)-*b*-poly(methylmethacrylate) (PS-*b*-PMMA) is an extremely well-studied model BCP system because the relative SFE of PS and PMMA is sensitive to annealing temperature. Between 170 and 270 °C, the SFE of both PS and PMMA is roughly equivalent (depending on composition). As this temperature range is below the degradation temperature of PS-*b*-PMMA (in a non-oxidizing environment) and is easily accessible by standard hot plates, it is relatively easy for this polymer system to form perpendicular structures when given an energetically neutral bottom interface[23,24]. A number of different neutral bottom interfaces for perpendicular assembly and DSA have been reported, including random co-polymer, brush, and other materials[22,25–30].

At both the top and bottom interfaces, the temperature range for neutral assembly depends in part on the relative proportion of PS to PMMA present. For example, in a lamellar system, the

proportion of PS to PMMA is equal, whereas for a cylindrical system, much more of the matrix (majority component) is present at the surface than the cylinders themselves (minority component). Therefore, different annealing temperatures are required to achieve neutral SFE for lamellae vs cylinders. For PS-*b*-PMMA cylinder forming materials discussed later in this thesis where PS was the minority component and PMMA was the majority, a relatively high annealing temperature of 270 °C was used[25].

1.6 Directed self-assembly: density multiplication

Another advantage of DSA is that the resolution of the chemical template can be much lower than the final resolution of the assembled BCP nanostructure. As DSA chemical templates are formed by lithography (EBL, 193i), using DSA with density multiplication is a way to enhance the resolution of a process beyond the tool capabilities.

For a cylinder-forming BCP in perpendicular assembly, the cylinders are hexagonally spaced at a pitch L_0. To generate a chemical template, a neutral copolymer mat is coated and patterned with spots spaced at some multiple of L_0. The spots are then plasma etched to remove the neutral mat, creating holes in the neutral mat. Those holes are then backfilled with a material preferential to the minority block (typically, a homopolymer brush) to complete template formation. Annealing the BCP on top of this pattern results in a single-orientation array of hexagonally packed cylinders guided by the underlying template. If L_0 is large enough (larger than the resolution limit of the EBL tool), it is technically possible to pattern the spots at 1:1 using EBL, with a spacing of L_0. However, for density multiplication, the spots could be patterned at $2L_0$, which would still result in the assembly of a single-orientation array of cylinders with a density multiplication factor of 4[10,16]. An illustration of 1:1 vs 1:4 density multiplication is shown in Figure 1.5.

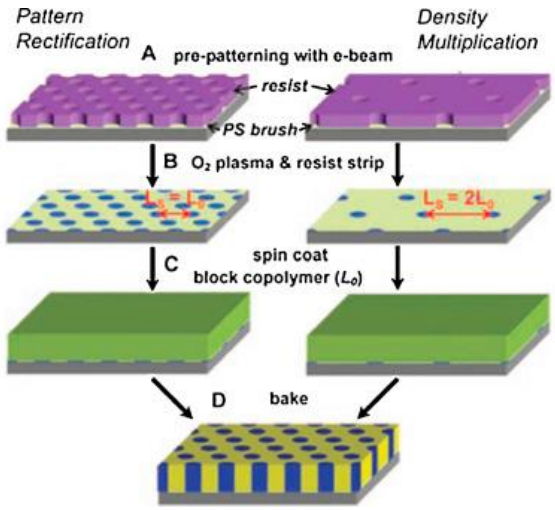

Figure 1.5 An illustration of 1:1 compared to 1:4 density multiplication. On the left, hexagonally packed spots are patterned at L_0, leading to 1:1 density multiplication, while on the right, spots patterned at $2L_0$ lead to 1:4 density multiplication. Taken from Science 321, 936–939 (2008)[16].

Each spot in a DSA chemical template is energetically preferential to the minority (cylindrical) block. In 1:1 DSA, each cylinder is registered to an underlying spot in the chemical template, hence 1:1. In 1:4 DSA, for each 1 preferential spot in the chemical template there are 4 aligned cylinders, hence 1:4. While only $1/4^{th}$ of the cylinders in 1:4 density multiplication are directly registered to an underlying spot in the chemical template, the thermodynamics and microphase behavior of the BCP results in the rest of the assembly being guided and anchored by those preferential spots. In this way, the resolution of the original pattern is quartered with a very narrow feature size distribution. The DSA pattern can be as large or as small as the chemical template can be written, from a few hundred nm^2 up to μm^2 in size. While perfecting a DSA process flow can be complex and challenging, no other lithographic technique is currently capable of producing such uniform, nanoscale features over large areas with so few process steps, which is why DSA lithography is such an appealing technique for both industrial and research devices.

1.7 Block copolymers and pattern transfer

Transferring the BCP microstructure into a technologically useful material like Si typically begins by the selective removal of one block. This step enables transfer of the BCP nanostructure via either deposition or etching, and is analogous to the development step in a conventional lithographic process. The process selectivity between the two blocks determines how the sacrificial block is removed. Blocks with highly orthogonal etch behavior (an etch that removes one block does not affect the other) are best suited for these processes. There are a number of different BCP pattern transfer approaches including direct pattern transfer, metal liftoff, and sequential infiltration synthesis.

Conventional lithographic approaches use the BCP itself as an etch mask, in which one block is removed via selective degradation. For example, the PMMA block of a PS-*b*-PMMA film selectively degrades upon UV exposure and can be rinsed away in an organic solvent, which leaves behind the PS nanostructure[31]. Similar results have been reported in other BCP systems with blocks vulnerable to UV radiation, such as polyisoprene-containing BCPs[4]. This technique has been successfully used to produce nanostructures templated by lamella, cylinder, and sphere forming PS-*b*-PMMA[16,32–34]. The disadvantages of this method include the volatility the organic solvents used to dissolve the degraded PMMA (typically, acetic acid), as well as collapse of high aspect ratio features due to the capillary forces endemic to wet etch processes.

Metal liftoff is a process option that can help improve etch selectivity prior to pattern transfer. In a metal liftoff process, one block is selectively removed from the BCP thin film structure. Then, a thin layer of metal (typically, Cr or Au) is deposited at a low temperature. The metal is deposited on the surface only in the areas where the sacrificial block was removed, replicating it. Then, a wet etch to remove the remaining block, and the metal on top of it, is done

to complete formation of a metal nanostructure, which can then be used as a template for dry etching with high selectivity[10,33,35,36]. Dry-etching with a plasma is an easier way of obtaining high aspect ratio features that are not subject to capillary collapse; however, the organic nature of most polymers makes it difficult to get large etch selectivity in a purely organic system. Converting the BCP template to an inorganic etch mask generally results in larger and more versatile process window for etching.

Choosing a BCP with a block containing an inorganic component is another way to achieve high block etch selectivity. This is typically accomplished either by synthesizing and directing the assembly of a BCP with an inorganic-containing block (such as for PS-*b*-PDMS), or by selectively decorating one block of a BCP with inorganic compounds post-assembly. This is a powerful approach because O_2 plasma has high etch selectivity for organic/inorganic systems, and can be used to completely remove an organic component while leaving the inorganic structure untouched. While a number of reports for inorganic post-modification of blocks have been reported, perhaps the most impactful is a technique called sequential infiltration synthesis[37–39].

Sequential infiltration synthesis (SIS) is a method that was developed at Argonne National Lab[40] to selectively introduce inorganic components into one block of a BCP film in order to improve the etch selectivity. In the SIS process, samples are typically placed in an atomic layer deposition (ALD) tool and subjected to precursors, as illustrated in Figure 1.6. In a standard ALD process, a reactive precursor is pumped into the chamber to saturate the surface, and then a second precursor (for thermal ALD, typically water) is pumped in to the chamber to react with the initial precursor to form (typically) a metal oxide monolayer. The process is repeated for some number of cycles (generally, tens to hundreds) to build atomically thin inorganic films monolayer-by-monolayer. However, in as SIS process, the initial volatile precursor is pumped into the chamber

and held for an extended period of time. This precursor diffuses into the BCP film and becomes selectively attracted to polar moieties in one of the blocks. The model system for SIS is forming alumina (AlO_x) in PS-*b*-PMMA, in which the precursor trimethyl aluminum (TMA) selectively accumulates at the carbonyl group in the PMMA block. After this diffusion step, the excess precursor is purged, and then water is pumped into the chamber to react with those adsorbed TMA molecules, nucleating AlO_x only within the PMMA domain[41].

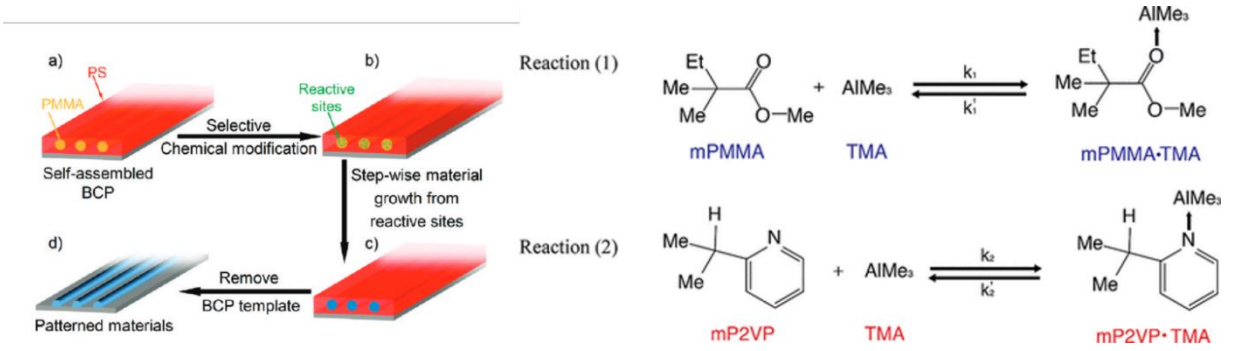

Figure 1.6 On the left, an illustration of the SIS process, showing how inorganic compounds are nucleated selectively within BCP domains for a PS-*b*-PMMA system. First, trimethyl aluminum is allowed to diffuse into the BCP film, and is then reacted with water vapour to nucleate alumina. This step is repeated for some number of cycles to build up alumina within the PMMA domain. Then, O_2 plasma is used to selectively remove the PS matrix, leaving only the alumina-impregnated PMMA domain, which can then be used as a template for pattern transfer. Taken from ACS Nano 5, 4600–4606 (2011).[41] On the right, proposed reaction kinetics for TMA complexation to PMMA and P2VP monomers. Taken from Chem. Mater. 32, 4499–4508 (2020)[42].

This process is typically repeated for 2-4 cycles to heavily impregnate the PMMA domain with inorganic AlO_x. After the SIS process, an O_2 plasma etch can be used to completely remove the PS block while leaving the inorganic PMMA-AlO_x structure unharmed, resulting in a highly precise and selective etch template for future pattern transfer. The number of cycles needed to build up sufficient alumina in the PMMA domain to form a continuous and robust template for pattern transfer depends on the ALD conditions (temperature, pump/purge time), the BCP (polymer type, film thickness), and the properties of the precursors[10,40,41]. SIS is a highly versatile

process that has been demonstrated for other polymer systems such as PS-*b*-P2VP, and for other inorganic materials including ZnO_x, TiO_x, SiO_x, SnO_x, VO_x, InO_x, GaO_x, and WO_x[40–42].

Significant progress has been made in understanding the mechanisms of SIS, improving its utility in BCP lithographic processes. The exact mechanisms by which the volatile precursors interact with the polymer chains in a SIS process have only recently been more carefully described. In its infancy, a common assumption in the field was that a simple, single-step reaction between the polymer and both precursors occurred to form the inorganic end product. However, recent reports show that the PMMA-TMA complex is unstable and sensitive to the TMA purge time after the exposure step. This behavior can likely be extended to apply to other ester carbonyl systems[43]. Recent computational reports suggest that the SIS mechanism occurs in three phases: (1) sorption of the precursor into the BCP film, (2) precursor diffusion through the film volume, and (3) complexation within the polymer. This behavior depends significantly on how well the polymer acts as a "sink" for the precursor. Most polymers are not perfect "sinks", so the reaction temperature becomes very important in determining the precursor diffusion, complexation, and AlO_x accumulation rate.

Recent work has shown that there is a thermal balance point (BP) where equal rates of precursor-polymer attachment and detachment occur, at which point maximum reactant accumulation can be attained. Below BP, the strong precursor-polymer binding hampers diffusion, leading to low reactant accumulation, while above BP the weak precursor-polymer binding prevents significant reactant accumulation. These new insights into the SIS process take it one step closer to being sufficiently well-characterized for widespread implementation in industrial processes. SIS has even been demonstrated as a way to increase the etch selectivity of resists[44].

Combining SIS with DSA is an extremely robust method for generating a perfect nanostructure and transferring it with high precision and minimal process drift into the materials of interest. BCP templated nanostructures using SIS have been successfully reported in a number of recent works, including ultrafiltraion and ultra-low thermal conductivity devices[25,45,46]. Of all the methods of pattern-transferring a BCP nanostructure into a material of interest, SIS is perhaps the most versatile because the polymer nanostructure can be directly used as a dry etching hard mask, and eliminating issues caused by capillary forces, liftoff defects, and etch selectivity.

1.8 Research applications of DSA-templated nanostructured devices

While BCP DSA has obvious applications in industrial lithography, the highly ordered nanostructures enabled by BCP templating also have many applications in nanostructured device research. DSA's ability to template complex, highly ordered nanostructures over large areas enables investigation of phenomena at dimensions previously unattainable by any other method. As research applications are typically low volume, the defect concentrations that currently impede DSA integration into high volume manufacturing is not a limiting factor. A vast number of prospective research applications for DSA-templated devices exist, including fabrication of complex optical metamaterials, liquid crystal displays, conductive polymer membranes, higher efficiency thermoelectrics, and ultra-low thermal conductivity materials.[3,25,45–50]

In this work, cylinder forming PS-*b*-PMMA was used as a template for fabricating ultra-nanoporous Si with ultra-low thermal conductivity. Low-thermal conductivity materials have become an increasingly active area of research due to heating issues that have arisen as device sizes continue to shrink. These materials can provide the needed thermal isolation to improve the function of devices like thermoelectrics and IR sensors. One method for reducing the thermal conductivity of a material is to introduce a periodic nanostructure capable of scattering heat carriers,

which are called phonons. Periodically nanostructured semiconductor materials, commonly referred to as phononic crystals, are thought to lower the thermal conductivity of the material by scattering phonons. In order for a material to scatter heat-carrying phonons effectively, the dimensions of the material must comparable in size to the phonons, typically <100 nm. DSA templated nanoporous materials provide the perfect solution for fabricating ultra-high porosity nanostructures with highly regular, defect-free feature sizes at the extremely small length scales required to affect thermal phonon transport.

1.9 Introduction to phonons

Phonons are a scientifically commonplace particle like photons or electrons, and are the particles by which sound and heat are transmitted through a medium. Like photons and electrons, phonons are considered to have both particle-like and wavelike characteristics. While there is a wealth of knowledge about how to manipulate photons and electrons in devices, devices designed to manipulate phonons are substantially less well developed. This is due to the fact that phonons are lattice vibrations and exist on an immense spectrum of frequencies as shown in Figure 1.7. At low frequencies (kHz), phonons are considered to be sound, while at high frequencies (THz), phonons are considered to be heat. The range of frequencies (and corresponding length scales) corresponding to each portion of the phonon spectrum is noteworthy. Audible sound comprises a range of frequencies from ~10^1-10^4 Hz, spanning ~3-4 orders of magnitude. The thermal portion of the phonon spectrum encompasses frequencies ranging from 10^{11}-10^{14+} Hz, another staggering 4 orders of magnitude. However, unlike for audible sound and ultrasound applications, which can be manipulated by structures on the centimeter to micrometer scale, nanoscale structures are required to manipulate thermal phonons.

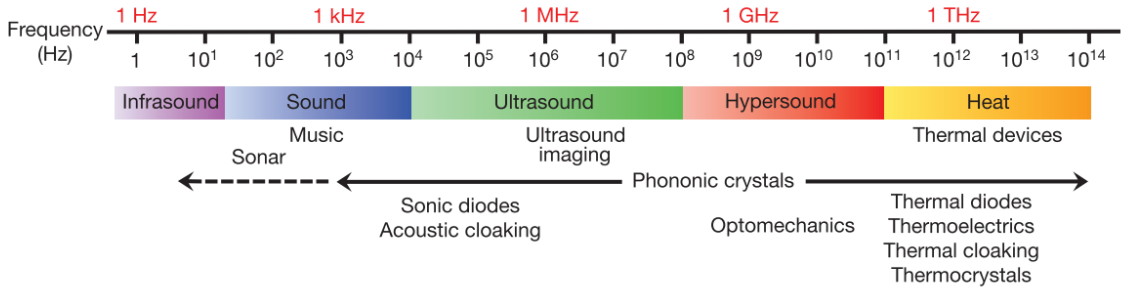

Figure 1.7 The spectrum of phonon frequencies spanning from infrasound, to audible sound, to ultra- and hypersound, to heat. The wide range of frequencies relevant to each portion of the spectrum makes phonon engineering challenging, particularly as the wavelengths approach tens to single nanometers. Figure taken from Maldovan et. al. *Nature* **503**, (2013).

There are a few main terminologies that are useful in describing the "size" of phonons, and by extension, the device dimensions needed to manipulate them: these are the phonon wavelength and mean free path (MFP) in a material. The MFP is the average distance that phonons in a given material will travel before undergoing a scattering event. For a given material, the available phonon wavelengths and corresponding energies are plotted to form a phonon dispersion relation. A simplified dispersion relation schematic, as well as a dispersion relation for Si, is shown in Figure 1.8. There are two main types of phonons (optical and acoustic), with longitudinal and transverse modes for each type. Typically, dispersion relations are either calculated or measured experimentally via inelastic neutron scattering. For thin film materials, dispersion relations are almost exclusively calculated because neutron transmission is very high and the signal to noise ratio is very low. For a material like Si, where heat transport is heavily correlated with the size of the material (i.e. thin film vs bulk), quantifying the exact wavelengths, MFPs, and energies of phonons in the system is challenging because they can't be directly measured[51]. Thus, the ability to accurately interpret experimental advances in thin film phonon engineering is limited by current understanding in computational models used to interpret that data. It is important to note that

discussions of phonon dispersion, wavelengths, MFPs, and energies in the forthcoming sections and thesis are entirely based on interpretation of experimental data by computational models.

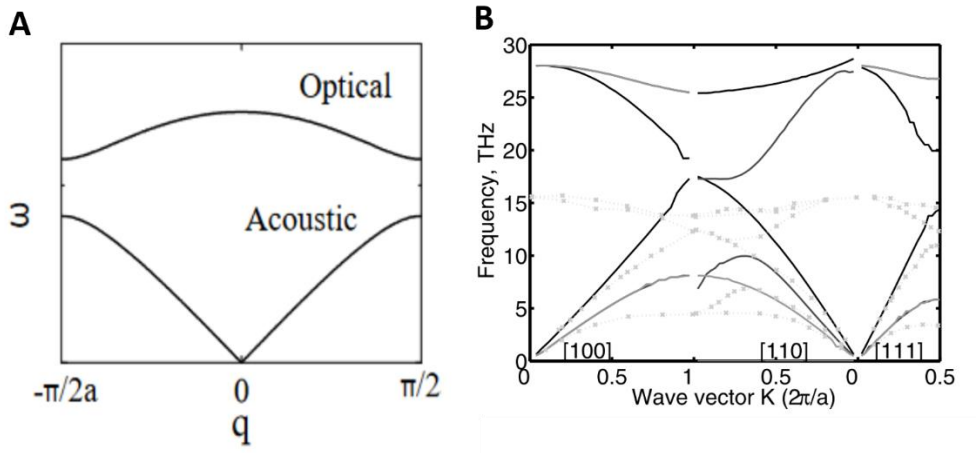

Figure 1.8 Illustration of phonon dispersion relations. In (A), a simplified schematic of a phonon dispersion is shown to illustrate optical and acoustic phonons[52]. In (B), an overlapped simulated and experimental dispersion relation for Si at 300K is shown. The solid lines are simulated values, and the dotted lines are experimental values[53]. Figures taken from Tsymbal, E. Y. Physics 927 Section 5: Lattice Vibrations and Eur. *Phys. J. B* **60**, 171–179 (2007).

A majority of computational phonon models are based on the Boltzmann transport equation (BTE), which is capable of predicting the dependence of thermal conductivity (among other parameters) on temperature, defects, and quantum confinement for a given material system. The BTE treats phonons as classical particles, which is typically valid in applications where the dimension of the system is larger than the spread of the phonon wave packet, and enables the definition of an average MFP [51,54]. In Si, thermal conductivity is thought to be dominated by phonons with MFPs larger than 100 nm, with the average MFP in bulk Si being approximately 300 nm (REFERENCE). However, phonons with MFPs ranging from 1-100+ nm also contribute to the thermal conductivity, with the significance of their relative contributions increasing as the size of the system shrinks[55].

Thermal phonon transport, which is analogous to heat flow, through a system can be categorized as either coherent or incoherent, depending on the relative length scales involved and whether the phonon behavior is wavelike or particle-like. In incoherent scattering, a phonon's phase and energy are not conserved after a scattering event, and heat tends to propagate diffusely. In coherent scattering, phonons are thought to undergo wave interference and scatter constructively or destructively with other phonons, as well as specularly from defects, boundaries, and other scattering centers. Under circumstances where the average MFP of the dominant heat carrying phonons is larger than the size of the system, the phonons can be described as travelling ballistically, or travelling very long distances before undergoing scattering.

In a bulk Si system in which the size of the material is much larger than the average MFP of thermal carriers, diffusive, incoherent scattering is typically an accurate way to portray and model phonon transport. However, it has been hypothesized that wavelike coherent scattering of phonons becomes significant as the size of the system shrinks down to the tens of nanometers in scale[56]. While coherent phonon scattering has been experimentally observed in a number of recent studies of nanostructured superlattice materials, recent reports support the emerging consensus that this effect may only be significant at very low (~0.5 K) temperatures, and quickly disappears at higher (ambient) temperatures[54,55,57–59]. At these extreme low temperatures, the phonon energies are significantly reduced and the wavelengths become sufficiently large for coherent interference and specular reflection from nanostructures. Emerging consensus in the field is that thermal transport in ambient conditions is likely dominated by diffuse, incoherent scattering events, and that coherent scattering is unlikely to play a significant role. However, many open questions about phonon transport, scattering mechanisms, and directionality in nanostructures at any temperature remain[46,60–62].

From either perspective, phonon transport through a solid is affected by a number of factors including the phonon frequency, the degree of crystallinity of the material, presence of interfaces, and material defects. Phonon scattering can be diffuse or specular, depending on the roughness and defectivity of the scattering center relative to the phonon MFP and wavelength. Phonons scatter from atomic-scale defects (vacancies, inclusions), interfaces (free surfaces, grain boundaries), and other phonons. High frequency (high energy) phonons tend to scatter easily and have relatively short MFPs, while lower frequency phonons tend to have longer average MFPs and are responsible for the majority of thermal conductance in a material[51]. Interfaces and boundaries in particular strongly affect phonon transport through a material, especially in the thin film regime. Phonons in a nanoscale system regularly encounter the free interfaces of the material, which significantly hinders phonon transport and reduces the thermal conductivity. Phonons also scatter strongly from surface roughness comparable to or larger to the phonon wavelengths. In nanoscale semiconductor devices, surfaces are typically sufficiently rough that diffuse boundary scattering significantly hampers phonon transport. The atomically smooth requirement for specular scattering in ambient temperatures is typically not met in these devices[51,54,55].

The relative contributions to thermal conductivity as a function of MFP can be computed for a given material, which is called the thermal conductivity accumulation (Figure 1.9)[54,63,64]. Thermal conductivity accumulation plots estimate which phonons are responsible for some percentage of thermal transport in a system. As seen for bulk Si in Figure 1.9, ~80 % of the thermal energy is carried by phonons with MFPs smaller than ~1 μm. In nanoscale devices, the relative contribution of short-MFP phonons to thermal conductivity is higher because longer MFP phonons tend to be scattered strongly at the surfaces[55]. Thus, for nanoscale semiconductor devices, phonon

engineering requires fabrication of structures in the single to tens of nm regime in order to most effectively cut off the majority of the spectrum of heat carriers.

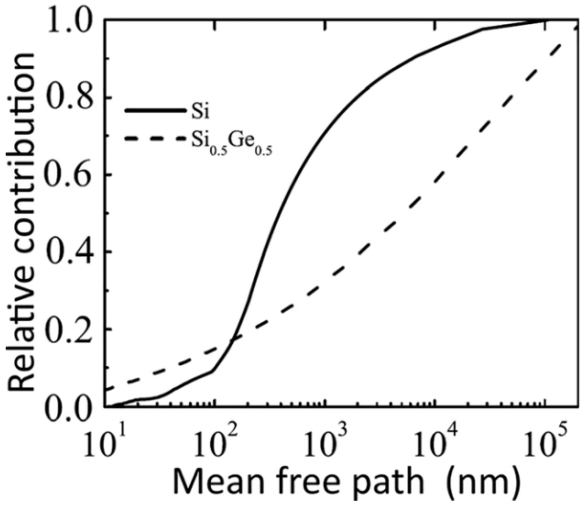

Figure 1.9 The relative contributions to thermal conductivity for bulk Si and SiGe plotted against MFP at room temperature. Taken from Appl. Phys. Lett. 109, 173104 (2016)[64].

1.10 Introduction to phononic crystals

Now that some of the basic properties of thermal phonons have been established, we can connect this knowledge to engineering devices that manipulate thermal phonons. As mentioned previously, heat management has become a significant issue in modern semiconductor devices, as dense arrays of nanoscale devices tend to have thermal management issues and suffer performance degradation as a result. One challenge in resolving the problem of thermal management is that nanoscale phonon transport is relatively poorly understood in systems where the material periodicity is comparable to the size of the phonons. Furthermore, as thermal phonons occupy such an immense range of length scales, with MFPs ranging from 1 nanometer to several micrometers, fabricating nanostructures to manipulate them is extremely challenging due to lithographic resolution limits.

Devices that manipulate phonon transport through a material are broadly called phononic crystals. Phononic crystals consist of a periodic array of one material inside a matrix of a different

material, where the two materials are elastically mismatched. Usually this is accomplished by creating a periodic array of voids (or holes, pores, etc.) in a thermally isolated material (such as Si) via nanofabrication. Typically, whether a periodic nanostructure scatters phonons and functions as a phononic crystal is assessed by measuring the thermal conductivity. If the thermal conductivity of the device is smaller than the expected reduction in thermal conductivity just by introducing voids alone, this is a good indication that phonons are being scattered by the device. The criteria for a nanostructure that reduces thermal conductivity to be classified as a "phononic crystal" are currently mechanistically broad. For example, conventional photonic crystals are periodic, dielectrically mismatched structures that manipulate photons as a function of wavelength to create photonic bandgaps, where specific wavelengths of light are prohibited from propagation. Photonic crystals are relatively easy to fabricate because the wavelengths of visible light are in the 400-800 nm range, which readily accessible by conventional lithography[65]. However, thermal phononic crystals with true bandgaps are very challenging to fabricate due to both the scale and frequency range of relevant thermal phonons. While thermal phononic bandgaps created via coherent scattering have been observed, such phenomena have been restricted to superlattice structures measured at ultra-low temperature (~0.5 K). In current literature, phononic crystal is a term that has been used to refer to any periodic nanostructure operating at any temperature in which thermal conductivity is reduced beyond volume reduction effects as a function of incoherent and/or coherent scattering. This can be confusing, and is an important distinction to be aware of.

1.11 Phononic crystal fabrication

A variety of phononic thermocrystals have been successfully fabricated and measured in recent reports. Generally, a phononic crystal device consists of a thin film material that has had periodic voids introduced into it through nanofabrication methods that is suspended over a void so

that it is thermally isolated from the base substrate. There are a number of reported strategies to fabricating such a structure, which often depend on how the thermal conductivity of the device will be measured.

Silicon phononic crystals are generally fabricated using silicon-on-insulator (SOI) wafers as the base substrate, which consist of a thin layer of monocrystalline silicon on top of a layer of silica (SiO_2) on top of a base (handle) Si wafer. The SiO_2 layer in a SOI wafer is usually a few hundred nanometers to a couple micrometers thick. The etch orthogonality of Si vs SiO_2 is well documented, as hydrofluoric acid (HF) selectively and rapidly etches SiO_2 without touching Si. The oxide layer provides mechanical support during the fabrication of the Si nanostructure in the top layer, and can be selectively removed via HF etching after the nanostructure fabrication is complete, thereby releasing the nanostructure from the base substrate and thermally isolating it.

Phononic thermocrystals must have nanoscale dimensions in order to lower the thermal conductivity of the base material. Various fabrication strategies have produced nanostructures with dimensions ranging from 14 nm to several micrometers in size. In general, EBL is used to fabricate samples with dimensions larger than ~80 nm, while more experimental techniques such as nanowire, microsphere, and BCP lithography have been used to fabricate devices with dimensions ranging from ~15-40 nm.

Important parameters describing the nanostructure are the pitch *p*, or center-center spacing of the holes; the porosity *P*; and then neck width *n*, or the width of the material remaining between two neighboring holes. The exact meaning of the pitch of a phononic nanostructure depends on the geometry of the device. For phononic crystals comprised of periodic voids in a thin film, lattices ranging from square, staggered square, hexagonal, to honeycomb have been reported, with void shapes ranging from circular holes, rough circular holes, to squares. Concentric arrays of

holes that possess a spectrum of pitches for heat lensing have also been reported, as well as nanowire arrays in which the pitch is defined as the wire-wire spacing. Examples of these device geometries are shown in Figure 1.10.

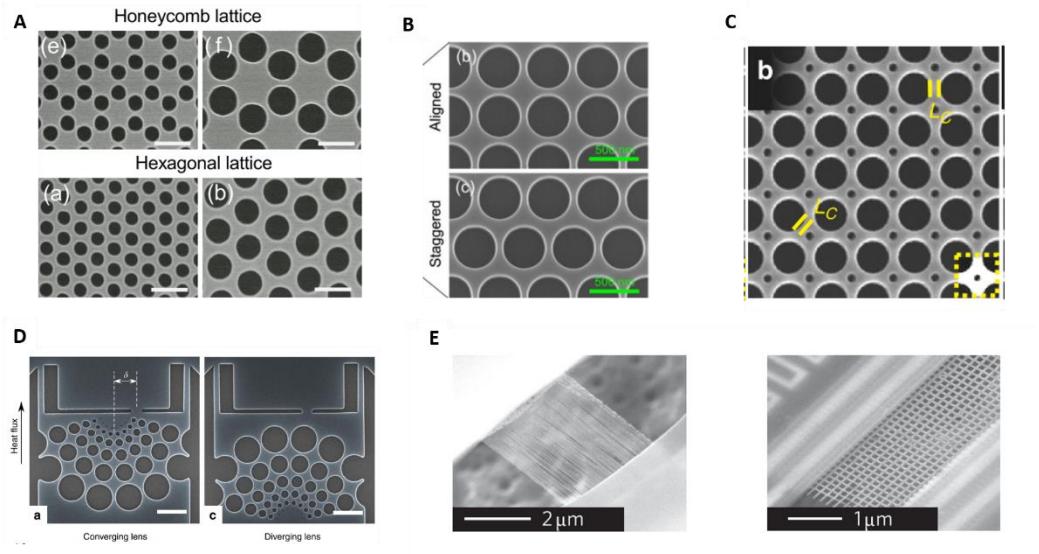

Figure 1.10 Examples of phononic crystals formed by introducing periodic voids with various geometries into Si. In A, hexagonal and honeycomb lattices are shown[60]. In B, square and staggered-square lattices are shown[66]. A staggered square lattice is not hexagonal; every other row is laterally shifted ½ the lattice constant. In C, an example of a phononic superlattice is shown, with two different hole sizes and lattice constants[67]. In D, an example of concentric arrays of holes for converging and diverging heat is shown[68]. In E, examples of square packed square holes (right) and a nanowire array (left) is shown[56]. All devices shown here, apart from the nanowire array, were fabricated via electron-beam lithography (EBL). Figures taken from *Nat. Nanotechnol*. **5**, (2010), *Phys. Rev. B* **93**, 45411 (2016), *Phys. Rev. B* **95**, 205438 (2017), *Nat. Commun*. **6**, 1–8 (2015), and *Nat. Commun*. **8**, 1–8 (2017).

1.12 Measuring the thermal conductivity of phononic crystals

There are a number of different ways to measure the thermal conductivity of a phononic crystal, which impacts the design of the device. Each method subject to its own measurement errors and interpretive biases. The majority of phononic crystals in recent literature have been measured by SiN_x MEMS devices or thermoreflectance.

SiN_x MEMS are relatively simple to fabricate, and consist of a pair of suspended (thermally isolated) SiN_x suspended membranes spaced at some set distance (~10-30 µm). SiN_x is the

material of choice for measurement apparatus like this due to its mechanical strength and low thermal conductivity. The SiN_x membranes are patterned with metallic heating and sensing coils, typically platinum. The phononic nanostructure is fabricated separately from the SiN_x measurement apparatus, released from its base substrate, then picked up and suspended between the two SiN_x membranes via micromanipulation techniques. The nanostructure is then wire bonded to the SiN_x membranes for thermal contact[56,69,70].

To measure the thermal conductivity, one of the SiN_x membranes generates heat, which travels through the suspended nanostructure and is sensed on the other side. The thermal conductivity is then calculated as a function of the contact resistance of the wire bond, the dimensions and cross-sectional profile of the nanostructure, and the various thermal and electronic material properties. While the SiN_x MEMS measurement approach is highly sensitive and can be used across a wide range of temperatures, monolithically fabricated Si structures cannot be measured using this approach as the supports must have low thermal conductivity. Thus, micromanipulation and wire-bonding are required, which can introduce mechanical defects and error into the measurement. These defects can make comparison between "identical" membranes challenging, making sensitive experiments difficult to interpret. Practically, it is also difficult to fabricate and measure high aspect ratio membranes (~10+) due to the required micromanipulation.

Thermoreflectance is another method for measuring the thermal conductivity of a material. Here, we will focus on time domain thermoreflectance (TDTR), which is the method used to measure our own devices[25,46]. For a TDTR measurement, a material that has a reflectivity that is very sensitive to changes in temperature is integrated into the nanostructure, typically in the form of an aluminum (Al) pad on top of the phononic nanostructure. Two lasers of different wavelengths are focused on an Al pad for heating and sensing. The pump laser heats the Al pad

in bursts while the probe laser continuously monitors the temperature-sensitive reflectivity. The heat generated by the pump beam dissipates through the nanostructure, causing the reflectivity of the Al pad to decay exponentially back to ambient. By heating Al pad and measuring the changes in reflectance over time, the thermal conductivity of the nanostructure can be extracted. TDTR measurements are typically done in a vacuum chamber to minimize thermal dissipation by convection, which ensures that the majority of heat dissipates along the device.

After the measurements are collected, the reflectivity signal is fit with a decaying exponential function to extract a decay constant. To use the decay constant to calculate the thermal conductivity of a device, a simulation is created, typically finite element method (FEM). The FEM simulations can be programmed with the device dimensions, geometry, and material properties, and used to simulate the decay times across a range of input prospective thermal conductivity values. The simulated thermal conductivity that produces a decay constant matching the experimentally measured constant is assumed to be the thermal conductivity of the real device. This simulation only accounts for the effects of phonon scattering in a material. Effective medium theories are typically applied to these computed values to account for volume reduction by introducing periodic voids. Thus, measuring the thermal conductivity of a device is a complicated effort involving computational interpretation of an experimentally measured value. The final reported values of thermal conductivity depend on the accuracy of the models, and are thus subject to variation between reports based on the physics of each individual model.

TDTR is limited in that it cannot be used to measure thermal conductivity of phononic crystals at ultra-low T (~0.5 K) because it relies on heating a material and monitoring the thermal dissipation. However, because TDTR can be performed non-destructively on any membrane featuring an Al pad, it is easy to fabricate monolithic top-down devices that do not require post-

fabrication manipulation. This eliminates the issues of micromanipulation and contact resistance found in the SiN_x MEMS approach, and facilitates comparison between similar devices fabricated simultaneously on the same chip. Vast numbers of virtually identical structures can be fabricated simultaneously, measured, and compared as a result, which is a throughput that is not possible with SiN_x MEMS measurements. As the structures are monolithically integrated, this method is also more compatible with high aspect-ratio structures, which is important for Si membranes due to its well-documented size-based thermal properties.

1.13 Current topics in phononic crystal research

While a number of authors have reported successful fabrication and measurement of phononic crystals with p and n values ranging from ~100 nm to >10 μm, significant lithographic challenges have limited the number of devices with $p \leq$ 50–100 nm. As thermal phonons in Si have MFPs ranging from single nanometers to micrometers, the most efficient thermal conductivity reduction strategy is to fabricate a nanostructure with a periodicity as close to the low end of that MFP range as possible. While doing so is lithographically challenging, recent progress has been made in fabricating ultrafine phononic nanostructures. Devices with $p \leq$ ~100 nm have been formed with p = 120 nm and n = 40–150 nm by EBL[60], with $p = 140$ nm by microsphere lithography[69], and with p of 36, 55, and 60 nm and n of ~20 nm by BCP lithography[62,69,71].

At present, much remains unknown about the precise mechanisms governing thermal phonon transport in nanostructured semiconductor materials. Major topics of discussion include whether coherent scattering (1) exists and (2) is a significant contributor to thermal conductivity in non-cryogenic temperatures. Studies arguing both for and against coherent phonon scattering in a variety of nanostructures across a range of temperatures exist, with result validity being a relatively open question due to most measurement techniques relying on some kind of heating.

While emerging consensus in the field appears to lean towards coherent scattering only being significant at extremely low T, it is difficult to conclusively disprove or prove due to the computational biases in measurement interpretation.

Another open question is whether the configuration of the periodic holes with respect to the primary direction of heat flow affects phonon transport, which has only recently begun to be studied in depth. There is a growing body of evidence to support the hypothesis that the directionality of phonons in a Si nanostructure can be significantly influenced by the parts of the nanostructure they "see", even at ambient temperatures[25,46,54,60,66–68,72,73]. Commonly, aligned lattices, in which a contiguous pathway through the nanostructure is parallel to the direction of heat flow, and staggered lattices, in which staggered holes are present in the path of heat flow, have been studied. However, these studies have generally been experimentally limited to nanostructures with *p* and *n* larger than 100 nm and 40 nm, respectively. As phonons easily scatter from defects, the nanostructures designed for these experiments must be defect-free and highly ordered. To date, reported ultrafine phononic nanostructures have not been defect-free, isoporous structures with tunable configurations[56,69,71], preventing this type of experiment from being done.

We present in this thesis an approach for using BCP DSA lithography to fabricate isoporous Si nanostructures with controllable orientation to probe the directionality of phonon transport at the nanoscale. Developing this process took ~5 years across two graduate theses. First, we will present a summary of previous work regarding phonon transport in silicon nitride. Then, we will present our original work in process development, fabrication, and thermal conductivity measurement of Si phononic crystals. As this research was done as part of an industrial collaboration with Panasonic, Japan, we will also present a summary of our work to fabricate an industrial prototype of a phononic crystal-enhanced IR sensor.

1.14 References

1. Stoykovich, M. P. *et al*. Directed assembly of block copolymer blends into nonregular device-oriented structures. *Science* **308**, 1442–1446 (2005).

2. Dolan, J. A. *et al*. Gyroid Optical Metamaterials: Calculating the Effective Permittivity of Multidomain Samples. *ACS Photonics* **3**, 1888–1896 (2016).

3. Dolan, J. A. *et al*. Optical Properties of Gyroid Structured Materials: From Photonic Crystals to Metamaterials. Adv. *Opt. Mater.* **3**, 12–32 (2015).

4. Dehmel, R. *et al*. Optical Imaging of Large Gyroid Grains in Block Copolymer Templates by Confined Crystallization. doi:10.1021/acs.macromol.7b01528

5. Lee, S., Bluemle, M. J. & Bates, F. S. Discovery of a Frank-Kasper sigma phase in sphere-forming block copolymer melts. *Science* **330**, 349–53 (2010).

6. Lee, S., Bluemle, M. J. & Bates, F. S. Discovery of a Frank-Kasper Phase in Sphere-Forming Block Copolymer Melts. *Science* (80-.). **330**, 349–353 (2010).

7. Martinez-Veracoechea, F. J. & Escobedo, F. A. The Plumber's Nightmare Phase in Diblock Copolymer/Homopolymer Blends. A Self-Consistent Field Theory Study. *Macromolecules* **42**, 9058–9062 (2009).

8. Frank S. Bates. Polymer Polymer Phase Behaviour. *Science* (80-.). (1991).

9. La, Y. H., Edwards, E. W., Park, S. M. & Nealey, P. F. Directed assembly of cylinder-forming block copolymer films and thermochemically induced cylinder to sphere transition: A hierarchical route to linear arrays of nanodots. *Nano Lett*. **5**, 1379–1384 (2005).

10. Ji, S., Wan, L., Liu, C.-C. & Nealey, P. F. Directed self-assembly of block copolymers on chemical patterns: A platform for nanofabrication. *Prog. Polym. Sci*. **54**–**55**, 76–127 (2016).

11. Matsen, M. W. & Bates, F. S. Block Copolymer Microstructures in the Intermediate-Segregation Regime. *J. Chem. Phys.* **106**, 2436–2448 (1997).

12. Han, E. et al. Perpendicular Orientation of Domains in Cylinder-Forming Block Copolymer Thick Films by Controlled Interfacial Interactions. *Macromolecules* **42**, 4896–4901 (2009).

13. Crossland, E. J. W. et al. A Bicontinuous Double Gyroid Hybrid Solar Cell. doi:10.1021/nl803174p

14. Daniel P. Sanders et al. Integration of Directed Self-Assembly with 193 nm Lithography. *J. of Photopoly. Sci. and Tech.* 11–18 (2010).

15. Stoykovich, M. P. et al. Directed Self-Assembly of Block Copolymers for Nanolithography: Fabrication of Isolated Features and Essential Integrated Circuit Geometries.

(2007). doi:10.1021/nn700164p

16. Ruiz, R. et al. Density multiplication and improved lithography by directed block copolymer assembly. *Science* **321**, 936–939 (2008).

17. Zimmerman, P. Double patterning lithography: double the trouble or double the fun? doi:10.1117/2.1200906.1691

18. Anisur Rahman, Javier Dacuna, Pinakpani Nayak, Gerald Leatherman & Stephen Ramey. Reliability studies of a 10nm High-performance and Low-power CMOS technology Featuring 3rd generation FinFET and 5th Generation HK/MG. *IEEE Proceedings* (2018).

19. Edwards, E. W. *et al*. Dimensions and shapes of block copolymer domains assembled on lithographically defined chemically patterned substrates. *Macromolecules* **40**, 90–96 (2007).

20. Hur, S.-M., Thapar, V., Ramírez-Hernández, A., Nealey, P. F. & De Pablo, J. J. Defect Annihilation Pathways in Directed Assembly of Lamellar Block Copolymer Thin Films. (2018). doi:10.1021/acsnano.8b04202

21. Maher, M. J. et al. Structure, Stability, and Reorganization of 0.5 L0 Topography in Block Copolymer Thin Films. *ACS Nano* **10**, 10152–10160 (2016).

22. Suh, H. S., Kang, H., Nealey, P. F. & Char, K. Thickness dependence of neutral parameter windows for perpendicularly oriented block copolymer thin films. *Macromolecules* **43**, 4744–4751 (2010).

23. Russell, T. P., Menelle, ' A, Anastasiadis, S. H., Satija, S. K. & Majkrzak, C. F. Unconventional Morphologies of Symmetric, Diblock Copolymers Due to Film Thickness Constraints. *Macromolecules* **24**, (1991).

24. Russell, T. P., Coulon, G., Deline, V. R. & Miller, D. C. Characteristics of the Surface-Induced Orientation for Symmetric Diblock PS/PMMA Copolymers. *Macromolecules* **22**, (1989).

25. Zhou, C. et al. *ACS Nano* 2020, 14, 6980−6989 doi:10.1021/acsnano.0c01463

26. Segal-Peretz, T. et al. Quantitative Three-Dimensional Characterization of Block Copolymer Directed Self-Assembly on Combined Chemical and Topographical Prepatterned Templates. (2016). doi:10.1021/acsnano.6b05657

27. In, I., La, Y.-H., Park, S.-M., Nealey, P. F. & Gopalan, P. Side-Chain-Grafted Random Copolymer Brushes as Neutral Surfaces for Controlling the Orientation of Block Copolymer Microdomains in Thin Films. (2006). doi:10.1021/la060748g

28. Langmuir, /, Han, E. & Gopalan, P. Cross-Linked Random Copolymer Mats As Ultrathin Nonpreferential Layers for Block Copolymer Self-Assembly. *Langmuir* **26**, 1311–1315 (2010).

29. Chang, T. H. et al. Directed self-assembly of block copolymer films on atomically-thin graphene chemical patterns. *Sci. Rep*. **6**, 1–9 (2016).

30. Mansky, P., Liu, Y., Huang, E., Russell, T. P. & Hawker, C. Controlling polymer-surface interactions with random copolymer brushes. *Science* (80-.). **275**, 1458–1460 (1997).

31. Thurn-Albrecht, T. et al. Ultrahigh-density nanowire arrays grown in self-assembled diblock copolymer templates. Science (80-.). **290**, 2126–2129 (2000).

32. Hong, A. J. et al. Metal Nanodot Memory by Self-Assembled Block Copolymer Lift-Off. **10**, 224–229 (2010).

33. Sunday, D. F. et al. Template-polymer commensurability and directed self-assembly block copolymer lithography. J. Polym. Sci. Part B Polym. Phys. **53**, 595–603 (2015).

34. Park, S.-M. et al. Directed Assembly of Lamellae- Forming Block Copolymers by Using Chemically and Topographically Patterned Substrates. *Adv. Mater.* **19**, 607–611 (2007).

35. Kim, S. O. et al. Defect structure in thin films of a lamellar block copolymer self-assembled on neutral homogeneous and chemically nanopatterned surfaces. *Macromolecules* **39**, 5466–5470 (2006).

36. Aligned nanowires and nanodots by directed block copolymer assembly | Enhanced Reader.

37. La, Y.-H., Stoykovich, M. P., Park, S.-M. & Nealey, P. F. Directed Assembly of Cylinder-Forming Block Copolymers into Patterned Structures to Fabricate Arrays of Spherical Domains and Nanoparticles. (2007). doi:10.1021/cm071208n

38. Jung, Y. S. & Ross, C. A. Orientation-controlled self-assembled nanolithography using a polystyrene - polydimethylsiloxane block copolymer. *Nano Lett.* **7**, 2046–2050 (2007).

39. Jung, Y. S., Jung, W. C., Tuller, H. L. & Ross, C. A. Nanowire conductive polymer gas sensor patterned using self-assembled block copolymer lithography. *Nano Lett.* **8**, 3777–3780 (2008).

40. Peng, Q., Tseng, Y. C., Darling, S. B. & Elam, J. W. Nanoscopic patterned materials with tunable dimensions via atomic layer deposition on block copolymers. *Adv. Mater.* **22**, 5129–5133 (2010).

41. Peng, Q., Tseng, Y. C., Darling, S. B. & Elam, J. W. A route to nanoscopic materials via sequential infiltration synthesis on block copolymer templates. *ACS Nano* **5**, 4600–4606 (2011).

42. Weisbord, I., Shomrat, N., Azoulay, R., Kaushansky, A. & Segal-Peretz, T. Understanding and Controlling Polymer-Organometallic Precursor Interactions in Sequential Infiltration Synthesis. *Chem. Mater.* **32**, 4499–4508 (2020).

43. Biswas, M., Libera, J. A., Darling, S. B. & Elam, J. W. New insight into the mechanism of sequential infiltration synthesis from infrared spectroscopy. *Chem. Mater.* **26**, 6135–6141 (2014).

44. Tseng, Y. C. et al. Enhanced polymeric lithography resists via sequential infiltration synthesis. *J. Mater. Chem.* **21**, 11722–11725 (2011).

45. Zhou, C. et al. FULL PAPER www.afm-journal.de Fabrication of Nanoporous Alumina Ultrafiltration Membrane with Tunable Pore Size Using Block Copolymer Templates. (2017). doi:10.1002/adfm.201701756

46. Tambo, N. et al. Ultimate suppression of thermal transport in amorphous silicon nitride by phononic nanostructure. *Sci. Adv*. **6**, eabc0075 (2020).

47. Li, X. et al. Perfection in Nucleation and Growth of Blue-Phase Single Crystals: Small Free-Energy Required to Self-Assemble at Specific Lattice Orientation. *ACS Appl. Mater*. Interfaces **11**, 9487–9495 (2019).

48. Martínez-González, J. A. et al. Directed self-assembly of liquid crystalline blue-phases into ideal single-crystals. *Nat. Commun*. **8**, 1–9 (2017).

49. Arges, C. G. et al. Interconnected ionic domains enhance conductivity in microphase separated block copolymer electrolytes. J. Mater. Chem. A **5**, 5619–5629 (2017).

50. Kambe, Y. et al. Role of Defects in Ion Transport in Block Copolymer Electrolytes. *Nano Lett.* **19**, 4684–4691 (2019).

51. Cahill, D. G. et al. Nanoscale thermal transport. *J. Appl. Phys.* **93**, 793–818 (2003).

52. Tsymbal, E. Y. Physics 927 Section 5: Lattice Vibrations.

53. Heino, P. Dispersion and thermal resistivity in silicon nanofilms by molecular dynamics. Eur. *Phys. J. B* **60**, 171–179 (2007).

54. Nomura, M., Shiomi, J., Shiga, T. & Anufriev, R. Thermal phonon engineering by tailored nanostructures. *Jpn. J. Appl. Phys*. **57**, 080101 (2018).

55. Cahill, D. G. et al. Nanoscale thermal transport. II. 2003-2012. *Applied Physics Reviews* **1**, 11305 (2014).

56. Yu, J.-K., Mitrovic, S., Tham, D., Varghese, J. & Heath, J. R. Reduction of thermal conductivity in phononic nanomesh structures. *Nat. Nanotechnol*. | **5**, (2010).

57. Ravichandran, N. K. & Minnich, A. J. Coherent and incoherent thermal transport in nanomeshes. *Phys. Rev. B - Condens. Matter Mater. Phys*. **89**, 205432 (2014).

58. Luckyanova, M. N. et al. Coherent phonon heat conduction in superlattices. *Science* (80-.). **338**, 936–939 (2012).

59. Ravichandran, J. et al. Crossover from incoherent to coherent phonon scattering in epitaxial oxide superlattices. *Nat. Mater.* **13**, 168–172 (2014).

60. Anufriev, R., Maire, J. & Nomura, M. Reduction of thermal conductivity by surface scattering of phonons in periodic silicon nanostructures. *Phys. Rev. B* **93**, 45411 (2016).

61. Hao, Q., Xiao, Y. & Zhao, H. Characteristic length of phonon transport within periodic

nanoporous thin films and two-dimensional materials. *J. Appl. Phys*. **120**, 065101 (2016).

62. Lee, J., Lim, J. & Yang, P. Ballistic Phonon Transport in Holey Silicon. *Nano Lett* **15**, 48 (2015).

63. Larkin, J. M. & McGaughey, A. J. H. Thermal conductivity accumulation in amorphous silica and amorphous silicon. *Phys. Rev. B - Condens. Matter Mater. Phys*. **89**, 144303 (2014).

64. Nomura, M., Nakagawa, J., Sawano, K., Maire, J. & Volz, S. Thermal conduction in Si and SiGe phononic crystals explained by phonon mean free path spectrum. *Appl. Phys. Lett.* **109**, 173104 (2016).

65. Li, W., Meng, F., Chen, Y., Li, Y. fan & Huang, X. Topology Optimization of Photonic and Phononic Crystals and Metamaterials: A Review. *Adv. Theory Simulations **2***, 1900017 (2019).

66. Verdier, M., Anufriev, R., Ramiere, A., Termentzidis, K. & Lacroix, D. Thermal conductivity of phononic membranes with aligned and staggered lattices of holes at room and low temperatures. *Phys. Rev. B* **95**, 205438 (2017).

67. Alaie, S. et al. Thermal transport in phononic crystals and the observation of coherent phonon scattering at room temperature. *Nat. Commun*. **6**, 1–8 (2015).

68. Anufriev, R., Ramiere, A., Maire, J. & Nomura, M. Heat guiding and focusing using ballistic phonon transport in phononic nanostructures. *Nat. Commun*. **8**, 1–8 (2017).

69. Tang, J. et al. Holey silicon as an efficient thermoelectric material. *Nano Lett*. **10**, 4279–4283 (2010).

70. Shi, L. et al. Measuring thermal and thermoelectric properties of one-dimensional nanostructures using a microfabricated device. *J. Heat Transfer* **125**, 881–888 (2003).

71. Takahashi, K. et al. Elastic inhomogeneity and anomalous thermal transport in ultrafine Si phononic crystals. *Nano Energy* **71**, 104581 (2020).

72. Maire, J. et al. Heat conduction tuning using the wave nature of phonons.

73. Tang, G. H., Bi, C. & Fu, B. Thermal conduction in nano-porous silicon thin film. *J. Appl. Phys*. **114**, 184302 (2013).

Chapter 2: Design, fabrication, and measurement of ultra-low thermal conductivity SiN_x phononic crystal membranes using block-copolymer directed self-assembly

Abstract

A summary of previous phononic crystal research in the group is presented in this chapter[1,2]. Studies have demonstrated that the thermal conductivity of crystalline semiconductor materials can be reduced by phonon scattering in periodic nanostructures that can be templated by self-assembled block copolymers (BCPs). Compared to crystalline materials, the heat transport mechanisms in amorphous inorganic materials are very different and have been explored far less extensively. In this work, we presented the design and fabrication of suspended amorphous silicon nitride (SiNx) membranes for the purpose of studying thermal conductivity in an amorphous solid. To form a periodic nanostructure, directed self-assembly (DSA) of cylinder-forming BCPs was used to pattern highly ordered, hexagonally close packed nanopores into the SiN_x with a pitch and neck width of 37.5 and 12 nm, respectively. Ultrafine nanostructuring with feature sizes below 20 nm enabled full suppression of the contribution of the propagating vibrational modes (propagons), leaving only the diffusive vibrational modes (diffusons) to contribute to thermal transport in SiN_x. The thermal conductivity of the suspended, nanoporous SiN_x membranes was 60% smaller than the classically predicted value based on the porosity of the suspended structure alone. These results demonstrated that the thermal conductivity of amorphous SiN_x can be reduced by introducing periodic nanostructures. The thermal conductivity reduction was explained as extremely strong diffusive boundary scattering of both propagons and diffusons. Changing the orientation of the hexagonal array of nanopores relative to the primary direction of heat flow had a smaller impact on amorphous SiN_x than was previously observed in monocrystalline silicon, suggesting that propagons are less likely to travel in straight lines in amorphous than crystalline materials.

2.1 Introduction

Amorphous thin films such as amorphous silicon nitride (SiN_x) are important materials in semiconductor devices[3] and are widely used in applications such as micro-electromechanical systems, transistors, and sensors. Managing the thermal properties of these materials as device dimensions continue to shrink has become an increasingly important engineering challenge[3–8]. Previously, our group conducted research on heat flow and thermal phonon behaviour in amorphous silicon nitride (SiN_x). While engineering the thermal conductivity of amorphous materials, particularly SiN_x, is highly essential for the thermal management of future electronic devices, compared to crystalline materials, the heat transport mechanisms in amorphous inorganic materials differ significantly and have been explored far less extensively[9]. Prior studies in the literature had demonstrated that the thermal conductivity (κ) of crystalline semiconductor materials could be reduced by phonon scattering in periodic nanostructures formed using templates fabricated both via e-beam lithography (EBL) and from self-assembled (SA) block copolymers (BCPs)[10–17]. These nanostructured membranes are called phononic crystals (PNCs). Therefore, we developed an original process for fabricating freestanding ultrafine nanoporous amorphous SiN_x membranes to study thermal conductivity in amorphous solids. While in SiN_x thin films, thermal transport is inherently impeded by the atomic disorder, the impact of periodic nanostructuring on (κ) was relatively less well explored both experimentally and computationally.

In theory, the Boltzmann transport equation (BTE), which assumes that phonons have a well-defined group velocity, could be applied to analyze amorphous systems. The BTE has been successfully applied to experimental studies on crystalline systems[18,19]. However, in amorphous solids, only a small portion of phonon vibrational modes are considered to have a well-defined group velocity. At the time of this study, the validity of the BTE as applied to an amorphous

system was an open question, which was important to answer in order to expand mechanistic understanding of the thermal behaviour in our amorphous SiN_X system. Previous computational models proposed that heat conduction in amorphous solids occurs via overlapping thermal energy between neighboring atoms, which vibrate independently[20–22]. Phonons in a fully disordered atomic lattice should therefore have extremely short MFPs, on the scale of the atomic spacing. More recently, work by Allen and Feldman suggested that vibrational modes in amorphous materials could be classified into three categories: propagons, diffusons, and locons[23–25]. Propagons are nonlocalized vibration modes at low frequencies and exhibit wave-like features. A large portion of the density of states are occupied by nonlocalized vibrational modes at higher frequencies called diffusons, which conduct heat in a diffusive matter over short distances. In this methodology, κ is expressed as a function of mode "diffusivity" to describe diffuson transport, whereas locons are localized vibration modes that do not contribute to κ.

Following this theory, several studies have focused on the properties of vibration modes in amorphous solids, for example, to define the threshold frequency between each of the three modes, the relative contribution of each vibrational mode to the total κ of a solid, and their size. Theoretical studies show that propagons, despite representing at most ~4% of phonons in an amorphous solid, contribute ~40% of the total κ of amorphous Si and that their mean free path (MFP) extends up to 1 μm[26,27]. Experimental studies had also shown that the cross-plane and in-plane κ depended on the feature size of the material[28–32]. Previous studies indicated that the thermal transport properties of amorphous solids could possibly be controlled via fine nanostructuring in analogy with those of crystalline materials, and scatter phonons like a PNC. These devices, which have been demonstrated in the form of nanowires, superlattices, and nanoporous PNCs, among many other variations of these systems, have been predominantly

achieved in crystalline materials[33]. At the time this study was conducted, it was unknown whether amorphous materials could be used to form a PNC, and much was still unknown about nanoscale thermal transport in these materials.

Our research into thermal phonon behaviour in SiN_x was partitioned into three general categories: (1), investigating the impact of EBL written holes with dimensions above 20 nm on κ, (2) designing a computational approach to predict the thermal behaviour of our system, and (3) measuring the impact of ultrafine nanopores with minimum feature sizes below 20 nm fabricated by BCP directed self-assembly (DSA) on κ. Theoretically, nanostructuring with a critical dimension smaller than the average MFP of the majority carrier would allow us to fully suppress contribution of the propagating vibrational modes (propagons), leaving only the localized diffusive modes (diffusons) to contribute to thermal transport in SiN_x.

In our computational and experimental research into nanostructured SiN_x, we found that κ of the nanoporous SiN_x membranes was 60% smaller than the classically predicted value based on just the membrane porosity. A combination of the phonon-gas kinetics model and Allen-Feldmann (AF) theory reproduced the measured results without any fitting parameters. The κ reduction was explained as extremely strong diffusive boundary scattering of both propagons and diffusons. We found that holes with much larger neck widths and pitches patterned by EBL lead to only a slight reduction in κ, which is closer to the classical porosity-based prediction. These results demonstrated that κ of amorphous SiN_x could be reduced by introducing periodic nanostructures that behave as a phononic crystal, where the relationship between the smallest dimension of the nanostructure and the length scale of the mean free paths (MFPs) of the dominant, heat-carrying phonons was critical[14,34,35]. Additionally, changing the orientation of the hexagonal array of

nanopores relative to the primary direction of heat flow had a less significant impact on amorphous SiN_x than was previously observed in silicon.

2.2 Experiment

To probe phonon behavior in amorphous SiN_x, thin film SiN_x membranes suspended over vacuum were fabricated using nanolithography techniques. Our starting substrate consisted of a low-stress SiN_x layer grown by LPCVD to a thickness of 70 nm on both sides of a 500 μm thick Si wafer (100 mm diameter). The samples were fabricated in a suspended membrane structure with a total length and width of 30 μm and 10 μm, respectively. Periodically spaced holes were etched completely through the SiN_x at pitches ranging from 36 nm to 1600 nm. EBL was used to fabricate samples at pitch sizes above 36 nm. BCP DSA was used to fabricate ultrafine 36 nm pitch phononic crystals. After hole etching, three 130 nm thick Al thermal contacts were deposited on each device: one in the center, and two larger pads at each end of the membrane. Next, a direct-write lithographer was used to pattern the shape of the membrane, and fluorine chemistry reactive ion etching (RIE) was used to cut the shape of the membrane into the SiN_x, exposing the underlying Si. Finally, the top SiN_x layer was suspended from the underlying Si by removing the Si under the bridge with anisotropic wet KOH etching. For the KOH to symmetrically etch away the Si underneath the SiN_x, the bridge was be rotated by 45° relative to the Si <110> direction, as shown in Figure 2.1. As a result, the fabricated, freestanding SiN_x membranes were suspended diagonally on top of a square, concave opening made of <111> Si sidewalls at 54.7° relative to the wafer surface.

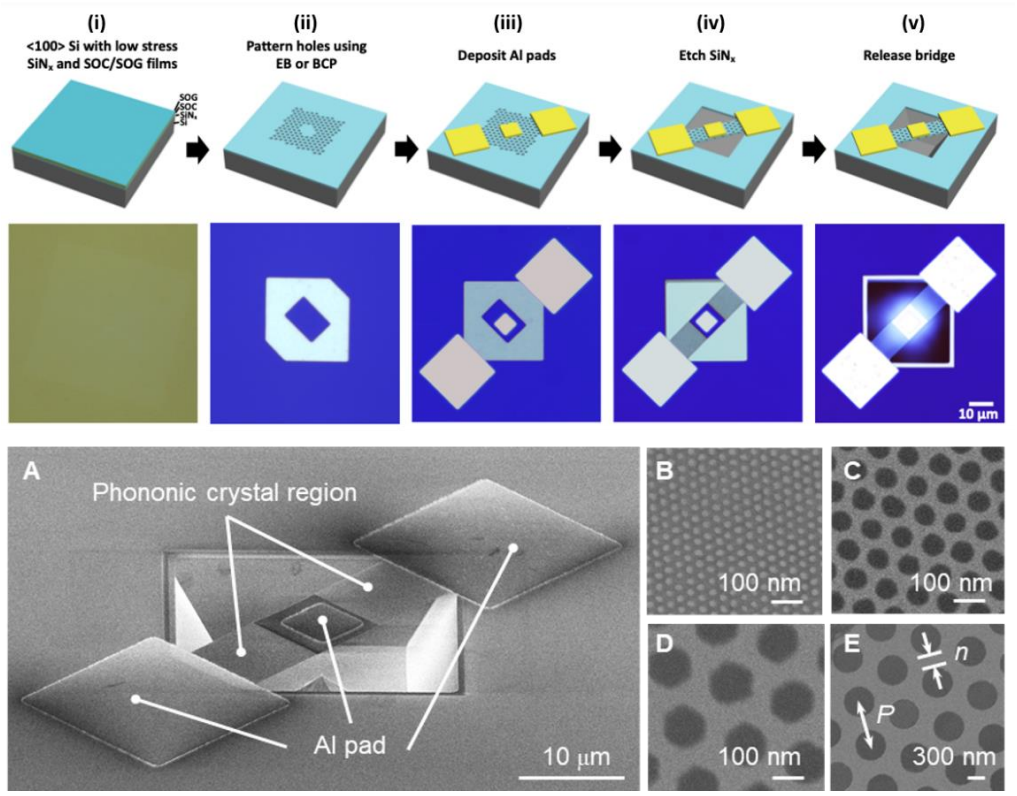

Figure 2.1 (i-v) Schematic illustration (top row) and corresponding optical microscopy images (middle row) of the fabrication process. (i) Initial Si substrate coated with SiN_x, spin-on-carbon (SOC), and spin-on-glass (SOG). (ii) Pattern transfer of the BCP-templated holes into the SOG/SOC film and the SiN_x layer. Only holes in the exposed area (light blue region in bottom row) were transferred into the SiN_x. (iii) Photolithography and metal lift-off were used to form the aluminum pads (white regions in bottom row). (iv) SiN_x was removed in the two triangular areas. (v) Wet etch of the underlying Si to release the SiN_x PNC membrane and leave it suspended above the opening in the Si. In the bottom panel, scanning electron microscopy (SEM) images of amorphous SiN_x phononic crystals are shown. (A) Overall image of a device. Al pads were deposited on the center and the edges of the suspended bridge for the thermal conductivity measurement. High magnification SEM image of the phononic crystal holes for pitch sizes of (B) 36 nm, (C) 100 nm, (D) 200 nm, and (E) 800 nm. The definition of pitch size *P* and minimum neck width *n* are illustrated in (E). Figure taken from ACS Nano 2020, 14, 6980−6989 (2020).

Time-domain thermal reflectance (TDTR)[16] was used to measure the thermal conductivity of the suspended nanoporous membranes. A two-color pump-probe diode laser system was used, consisting of a pump and probe laser. Both lasers irradiated the central Al pad, and the transient response of heat dissipation through the amorphous SiN_x membranes was measured to obtain κ. A

detailed description of our TDTR measurement technique is included in references 1 and 2, as well as in Chapter 5.

2.3. Ultimate suppression of thermal transport in amorphous silicon nitride by phononic nanostructure

The as-measured material thermal conductivity κ_{mat}, which did not account for effects caused by porosity, of all membrane geometries is shown in Figure 2.2[1,2]. The κ_{mat} of the nonporous membrane was 2.5 ± 0.2 W/mK, which agreed with previously reported values[6]. For the nanoporous PNC membranes, we observed a clear decrease in κ_{mat} with decreasing neck width *n*, which became particularly steep when *n* decreased below 20 nm. We also computed the surface to volume ratio s/v of each membrane geometry and found that κ_{mat} also decreased with increasing s/v ratio. This was likely due to boundary scattering becoming more prevalent as the s/v ratios increased, which disturbed long-MFP carriers like propagons[36]. Since propagons account for a substantial proportion of thermal transport in amorphous SiN_x, the strong reduction in κ_{mat} was likely caused by enhanced boundary scattering of propagons. Interestingly, we observed in Figure 2.2B that κ_{mat} converged to a value of ~ 1 W/mK after a monotonic decrease when the s/v ratio increased above 0.1 nm^{-1}. This indicated that the propagons were fully suppressed, leaving only the diffusons to contribute toκ; diffusons have much shorter MFPs than propagons and thus were less affected by nanostructuring. We called this convergence threshold the "diffusive limit," as this κ represented the contributions of diffusons alone. These initial results demonstrated that nanoporous SiN_x membranes could function as PNCs and successfully modify κ_{mat}.

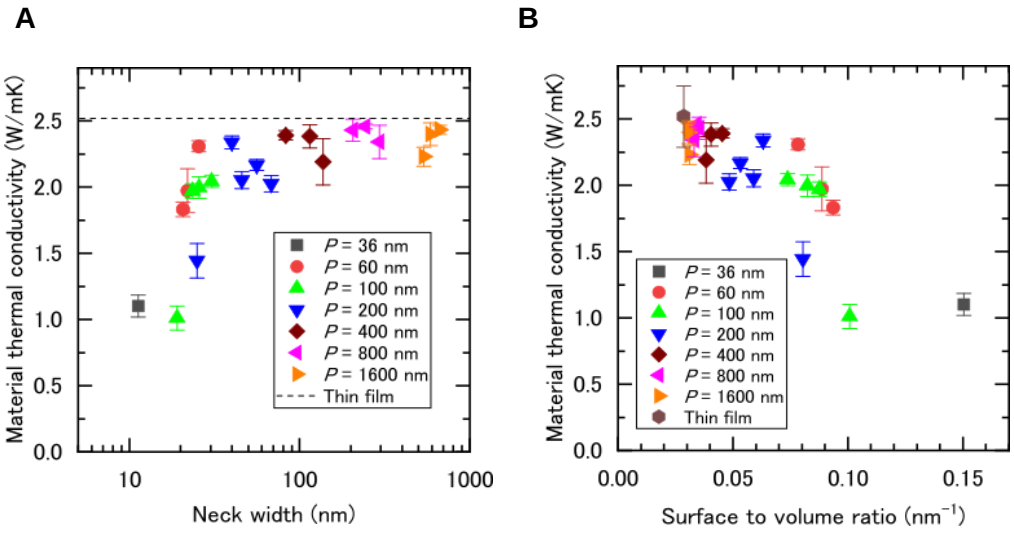

Figure 2.2 Material thermal conductivity of amorphous SiNx phononic crystals. Material thermal conductivity κ_{mat} of amorphous SiNx thin films plotted as a function of (A) the minimum neck width and (B) the surface-to-volume ratio. Plot legends denote the pitch size of PNCs. The dashed black line in (A) represents the thermal conductivity of the nonporous amorphous SiNx thin film. Figure taken from *Sci. Adv.* **6**, (2020).

To probe the mechanisms behind κ in our PNCs, we conducted simulations to predict the relative contributions of the propagons and diffusons to κ (κ_P and κ_D respectively) in our material system. First, we calculated the bulk thermal conductivity of SiN_x, which found κ_{mat} to be 2.9 W/mK, a value consistent with those measured by Sultan et al.[37], Zink and Hellman[38], and Hossein et. al.[39]. The calculated κ_P and κ_D were identified as 1.8 W/mK and 1.1 W/mK, respectively. This indicated that propagons with long MFPs could contribute to a significant part (62%) of the κ_{eff} of bulk SiN_x, which was consistent with the work reported by Sultan (50%)[30]. Details of this calculation are included in references 1 and 2**.**

After validating our model for calculating the bulk κ, we computed the thermal transport properties of nonporous SiN_x thin film membranes. The effects of boundary scattering (at pore walls and surfaces) were applied to the bulk model using Monte-Carlo Ray Tracing (MCRT), which had successfully used in previous studies[38] on crystalline solids. The MCRT method allowed us to compute the effective MFPs of propagons and diffusons in nonporous SiN_x

membranes, which then allowed us to predict the magnitude of κ. By this method, we calculated κ at 300 K, κ_T, of the nonporous membranes to be 2.3 W/mK, which was comparable to our experimentally measured value of 2.5 ± 0.2 W/mK. Propagon scattering at boundaries resulted in the 21% reduction in κ relative to the bulk value for SiN_x. Diffusons, however, were not noticeably affected by the increased surface area of the thin film membranes because of their very short (angstroms to a few nanometers) MFPs. Therefore, κ_D of bulk SiNx and κ_D of the nonporous thin film membrane were both 1.1 W/mK. These values were in agreement with our diffusive limit (1.01 ± 0.09 W/mK). These results supported our hypotheses that propagons could be dramatically suppressed by nanostructuring, and that κ would be dominated by diffuson contributions when n < 20 nm.

Next, we calculated κ_{eff} for the nanoporous PNC membranes. We applied the Maxwell-Garnett (MG) effective medium model to our experimentally measured values of κ_{mat} to account for the volume reduction effect of introducing porosity, written as $\kappa_T = \frac{1-\varphi}{1+\varphi}\kappa_{mat}$ where ϕ is the porosity. We verified that the MG model was germane to our system using the steady state thermal analysis module of ANSYS. Relative to the nonporous membranes, we found that the values of κ_{eff} in our nanoporous PNC membranes were significantly reduced, which had a lowest measured value 0.26 ± 0.03 W/mK (Figure 2.3). It is worth noting that our experimentally measured and simulated values for all membranes were within 10% of each other, which indicated that our model accurately depicted κ of amorphous PNCs.

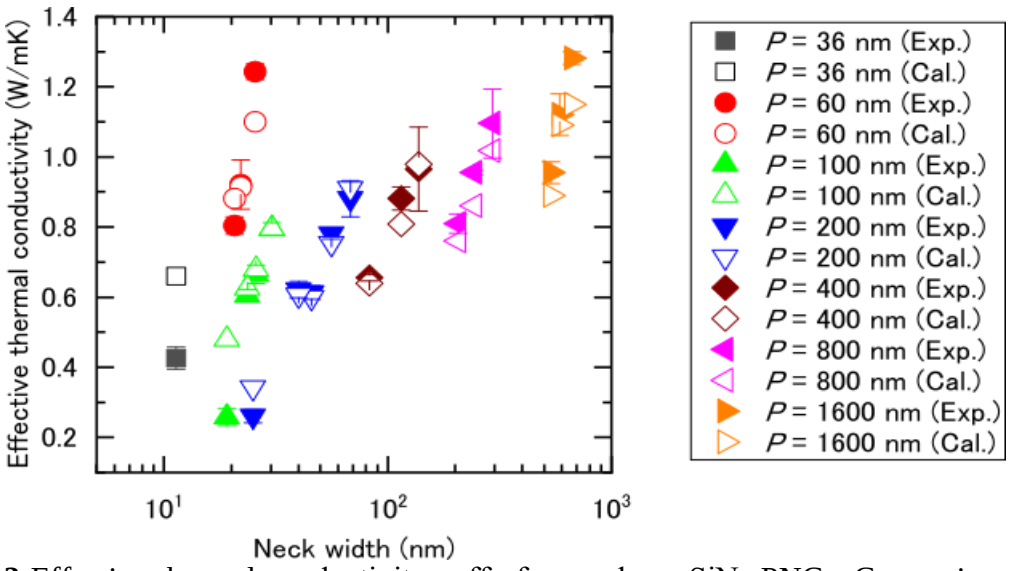

Figure 2.3 Effective thermal conductivity κeff of amorphous SiN_x PNCs. Comparison between the measured and the simulated effective thermal conductivity amorphous SiNx PNCs plotted as a function of the neck width. Plot legend denotes PNC pitch size. Figure from *Sci. Adv.* **6**, (2020).

In Figure 2.4A, we show how reducing the MFPs of propagons and diffusons affected κ_D and κ_P. By introducing periodic nanostructures into the SiN_x, we were able to reduce the κ spectra of propagons and diffusons by 90% and 80%, respectively, relative to bulk. Quantitatively, κ_P, κ_D, and κ_T were reduced to 0.15 W/mK, 0.19 W/mK, and 0.34 W/mK, respectively, which was almost one order of magnitude smaller than κ_P (1.1 W/mK), κ_D (1.8 W/mK), and κ_T (2.9 W/mK) we calculated for bulk SiN_x. Boundary scattering played a significant role in these reductions: even for samples with a large *n* of 665 nm, the reduction in κ_P exceeded 70%. The percentage of scattered propagons rose to 90% when *n* decreased below 20 nm. Boundary scattering was also demonstrated to affect diffuson propagation, where, depending on *P* and *n*, 40-80% reduction in κ_D was observed. This demonstrated that even short-MFP (0.5-10 nm) diffusons are subject to boundary scattering in an ultrafine nanostruature. Thus, nanostructured amorphous solids are able to function as PNCs, in which heat carriers are significantly scattered across a wide range of MFPs.

Our calculations demonstrated that κ could be described well by the particle-based BTE. Results from this model suggested that there was no fundamental difference between diffusons and propagons when considering boundary scattering in this application. Furthermore, the results suggested that for SiN_x PNCs measured at ambient temperatures, coherent phonon behaviour is not a significant contributor to low κ. We believe that this would change with decreasing temperature, as observed for crystalline PNCs[40], where low frequency phonons have a more significant role in heat transport.

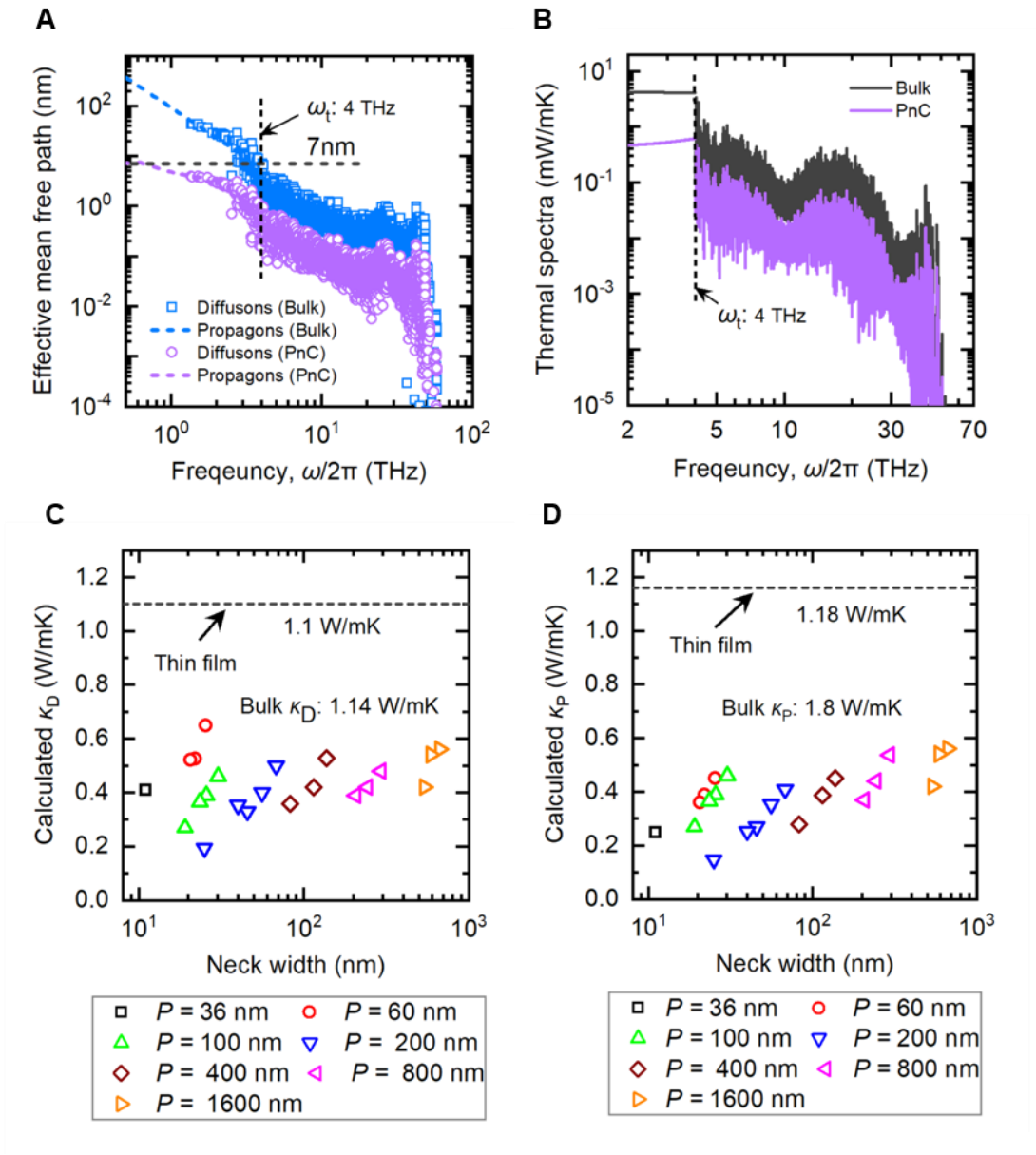

Fig. 2.4 Calculated thermal properties of amorphous SiN_x. (**A**) Comparison of the effective mean free path of propagons and diffusons for bulk SiN_x and SiN_x phononic materials, taking the sample with pitch size *P* of 200 nm and hole diameter *D* of 175 nm as an example. (**B**) Comparison of thermal conductivity κ spectra for bulk SiN_x and SiN_x phononic materials, taking the sample with *P* = 200 nm and *D* = 175 nm as an example. (**C**) and (**D**) are the calculated thermal conductivity contribution from diffusons (κ_D) and propagons (κ_P) for all samples as a function of neck width *n*. Figure from *Sci. Adv.* **6**, (2020)

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2.4. The use of directed self-assembly of block copolymers to fabricate phononic crystals in amorphous silicon nitride, resulting in enhanced thermal conductivity reduction

In this section, the thermal conductivity results from the 36 nm pitch membranes, which were fabricated using BCP templates, are described in greater detail[1,2]. As discussed in the previous section, the nature of heat transport, and thereby phonon transport, in amorphous solids is relatively complex and poorly understood compared to crystalline systems. Given the minute length scales of the MFPs relevant for heat carriers in SiN_x, it logically follows that such carriers would be more strongly affected by a nanostructure with minimum dimensions on the order of 10 nm. Nanostructures at this length scale are difficult, if not impossible, to achieve with modern top-down lithography techniques due to resolution limits of EBL and photolithography. However, it is possible to fabricate nanostructures with long-range order at very small length scales via block-copolymer assembly[41]. Applying BCP DSA to conventional lithographic techniques provides a robust method to fabricate high-precision nanostructures, such as PNCs, in inorganic materials.

Our work in using BCP DSA to fabricate ultrafine nanostructured membranes built on previous work in which BCPs were used to template PNCs. Lim et al. used self-assembled, cylinder-forming polystyrene-block-poly(2-vinylpyridine) to etch holes into thin films of monocrystalline silicon[14,34,42]. The resulting nanoporous ("holey") silicon membranes had a hole pattern with a pitch *p* of ~60 nm and neck *n* in the range of 16–34 nm. These nanostructures were

shown to scatter thermal phonons, resulting in significantly reduced κ_{eff} values. However, the self-assembly of the BCP used to form the initial pattern inherently created grain boundaries and other defects; as phonon scattering can be heavily influenced by grain boundaries, rough interfaces, and pattern defects, it was difficult to separate the effects of the nanostructures from those of the defects and interfaces on the reduced κ_{eff}. In our work, we built on their results in two ways: (1) by decreasing the pitch from 60 nm to 36 nm, and (2) by eliminating all defects by guiding the assembly of the BCP using DSA. This defect-free fabrication approach also allowed us to probe the effects of nanostructure geometry on the phonon transport.

To fabricate arrays of nanopores with long-range (hundreds of μm) order from SiN_x thin films, we used the same fabrication approach we used to make EBL-patterned holes at larger pitches. To perform DSA, an additional step was required, and e-beam was used to pattern a chemical template that was an array of hexagonal spots spaced at twice the L_0 of the BCP (Fig 2.5). The chemical template was able to subsequently direct the self-assembly of cylindrical domains of the BCP into large, defect-free two-dimensional patterns. We then etch-transferred the BCP pattern into the underlying SiN_x using a stack of spin-on-carbon (SOC) and spin-on-glass (SOG) on top of the SiN_x film (Fig 2.5 a). The combination of SOG and SOC layers is commonly used in pattern transfer processes in high volume manufacturing because it can provide a highly selective dry etch process, with fluorinated and oxygen-rich plasmas selectively etching SOG and SOC, respectively. The resulting nanoporous SiN_x membranes had long-range, defect-free, hexagonal close-packed (HCP) holes with small *p* and *n* (37.5 and 12 nm, respectively). It is worth noting that the BCP used for these experiments was identical to the BCP mentioned in Section 2; the difference in pitch was due to slight calibration differences between our SEM and that of our

collaborators'. See Chapters 1, 3, and 5 for additional details about this block copolymer, self-assembly, and DSA process.

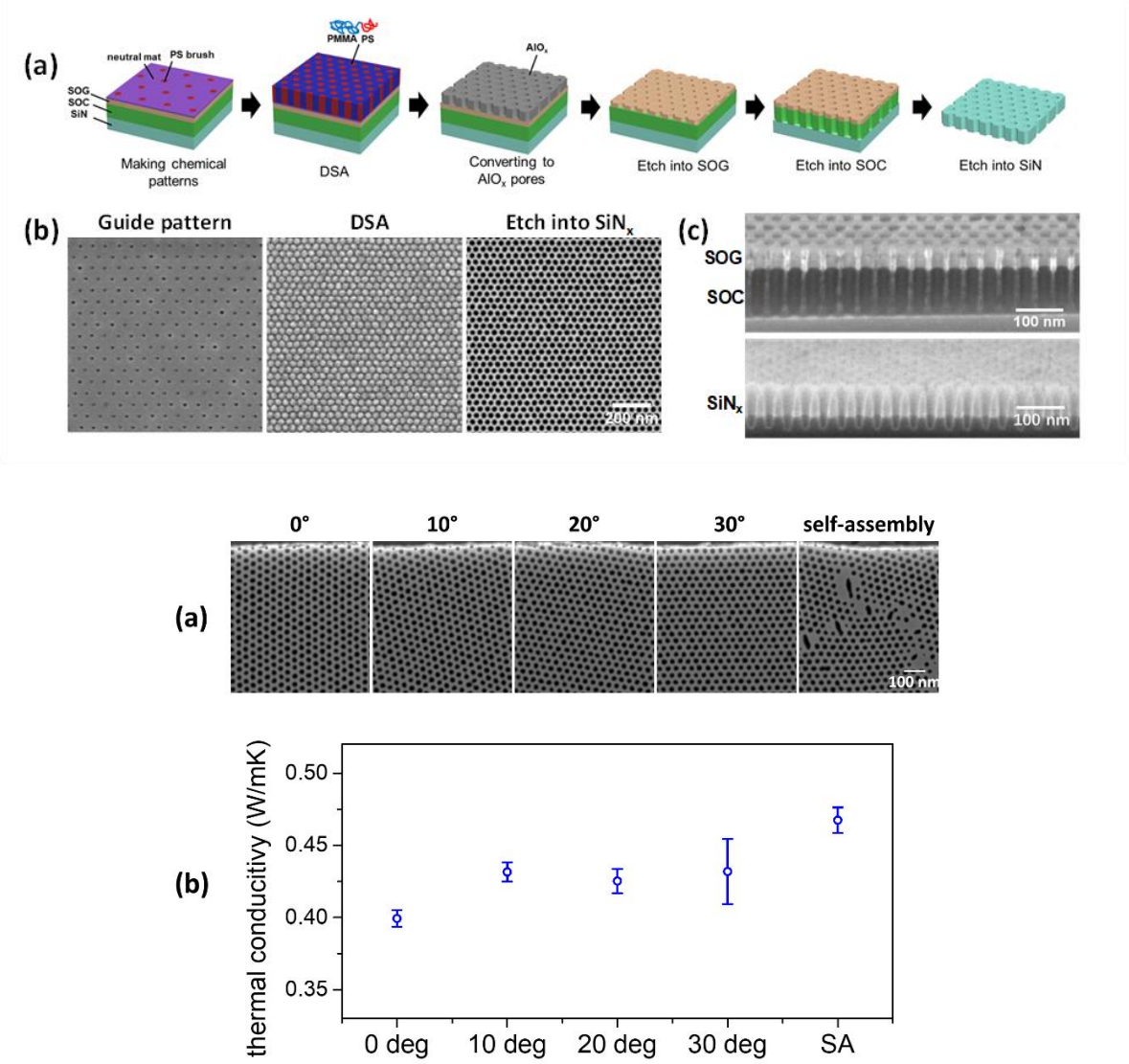


Figure 2.5 (a) SEM images and **(b)** corresponding thermal conductivities of DSA patterned silicon nitride phononic crystals with four different rotation angles and of self-assembled (SA) holes. The SEM images were taken near the longer edges of membranes. The white arrow in **(a)** at 0° shows the direction of heat flow. Figure from ACS Nano 2020, 14, 6980−6989 (2020).

The BCP DSA patterned membranes were measured in TDTR as described previously. The results of these measurements, compared to EBL-patterned 800 nm pitch and nonporous membranes is shown in Table 2.1. The DSA patterned PNC had the smallest κ_{eff}, which was 61%

smaller than the value of the nonporous membrane. This reduction in κ_{eff}, as discussed previously, was due to both volume reduction and propagon scattering at boundaries. Because the percent reduction in κ_{eff} relative to the nonporous film was only 8% smaller for the 800 nm pitch sample, but was 61% smaller for the DSA sample, we concluded that volume reduction alone could not be the only contributing factor to κ_{eff} reduction. Because amorphous materials lack the translational symmetry and periodicity of an atomic lattice, conventional concepts of phonon transport in crystalline materials do not necessarily apply directly to amorphous materials[1]. However, we observed that the effect of our nanostructures on the thermal properties of our amorphous SiN_x membranes was similar to observations in crystalline materials. The PNC membranes with smaller *p* and *n* had smaller κ_{eff} than the nonporous films, even after taking volume reduction into account[3]. Thus, our work here suggested that propagons with long MFPs were scattered by the porous nanostructures, which resulted in a decrease in κ_P (and by extension, κ_{eff}) that far exceeded the decrease caused by porosity alone.

	p **(nm)**	***D*** **(nm)**	***n*** **(nm)**	**Porosity (%)**	**τ (μs)**	$\kappa_{predicted}$ **(W/mK)**	κ_{eff} **(W/mK)**
DSA holes	37.5	25.5	12.0	41.9	570 ± 30	1.0	0.39 ± 0.02
e-beam holes	800	476.9	323.1	32.2	210 ± 4	1.3	1.2 ± 0.02
Nonporous	0	0	0	0	120 ± 5	2.5 ± 0.1	2.5 ± 0.1

Table 2.1 Summary of the dimensions of the nanoporous membranes and the thermoreflectance measurements. *p*, *d*, and *n* represent nanopore pattern pitch, nanopore diameter, and neck width between nanopores, respectively. τ is the decay time of the thermoreflectance measurement. $\kappa_{predicted}$ and κ_{eff} are the thermal conductivity values based on the classical porosity and on the analysis of the thermoreflectance measurement, respectively.

We compared changes in κ_{eff} with respect to *n* between the 800 nm pitch and DSA sample to qualitatively estimate the MFP distribution of propagons[43]. The EBL patterned sample with *p* = 800 nm and *n* = 323 nm exhibited only an 8% reduction in κ_{eff} beyond the effect of porosity, indicating that propagons with MFPs greater than 323 nm contributed little to heat transport. In

contrast, DSA-patterned SiN_x with p = 37.5 nm and n = 12 nm decreased κ_{eff} by 61%, which showed that a large proportion of propagons were scattered at this length scale. We believe the incoherent and diffuse scattering of phonons was the dominant cause of these reduced κ_{eff} values.

Due to the high precision, defect-free nature of our DSA process, we were also able to probe the effect of nanostructure geometry on the κ_{eff} of SiN_x. As mentioned in Chapter 1, it has been established that varying nanostructure geometry along the path of heat transport can impact phonon transport, and therefore the κ of a nanostructured crystalline material like Si[34,35,44]. For geometries with a line-of-sight pathway through the nanostructure parallel to the direction of heat flow, κ_{eff} would be higher than for a nanostructure with a blocked pathway. To probe whether this effect could occur in an amorphous material like SiN_x, we rotated the orientation of the DSA pattern with respect to the long axis of the membranes to change the pathway "seen" by the phonons (Figure 2.5). For a pattern orientation of 30°, the line-of-sight pathway was parallel to the direction of heat flow, while rotating the pattern orientation to 0° resulted in the line-of-sight pathway being orthogonal to the direction of heat flow, and thus obstructed. Paths with varying degrees of open-ness (10°, 20°) were also fabricated, as well as a polycrystalline self-assembled structure with random grain (and thus pathway) orientation. The results of the measurements on all geometries are shown in Figure 2.5.

While we did observe that κ_{eff} of the 0° sample was the smallest, it was less than 10% smaller than κ_{eff} the other three lattice orientations. Thus, we did not observe the change in the orientation of the SiN_x PNC to have a significant impact on κ_{eff}. The κ_{eff} of the self-assembled BCP membrane was about 17% higher than that of DSA sample at 0°, and 9% higher than those of the samples at 10°, 20°, and 30°. These differences were probably a result of structural irregularities

at grain boundaries, where larger nonporous regions of SiN_x exist and could contribute to heat conduction.

2.5. Conclusions

We presented a strategy to fabricate amorphous SiN_x membranes that behave as PNCs, for which κ_{eff} can be measured via thermoreflectance. We developed a robust fabrication process to create nanoporous thin film SiN_x membranes at a large range of pitches, neck widths, and porosities. Our experimental results could be examined in two parts: EBL patterned samples at large pitch, and BCP DSA patterned samples at a pitch of 36-37.5 nm. Notably, the DSA method, which results in defect-free nanostructures over large areas, enabled us to probe phonon behavior at length scales below the traditional resolution limits of modern lithography equipment. Using TDTR to measure κ_{eff} of these membranes, we showed that nanostructuring is a viable approach to manipulate κ_{eff} of amorphous materials.

Additionally, we demonstrated the ability to computationally obtain κ_{eff} of bulk, thin-film nonporous, and micro- and nanoporous amorphous SiN_x. By defining the MFPs of propagons and diffusons using the kinetic gas model and AF theory, the measurement and analysis of the thermal conductivities of the SiN_x membranes was robust and reproducible without requiring any fitting parameters. From these computations, we learned that the MFPs of both propagons and diffusons are suppressed by boundary scattering in the nanoporous membranes, particularly for smaller *p* and *n* samples, resulting in significant decreases in κ_{eff}.

While a number of previous studies have considered coherent wave scattering as a possible mechanism behind thermal conductivity reduction in nanostructured thin films, we believe that coherent scattering likely did not play a role in room-temperature measurements presented in this work. The coherent effect likely only applies when (1) the surface is atomically

smooth, minimizing diffuse scattering at the interface, and (2) when the period of the holes is on the same scale as the phonon wavelength, which is typically on the order of a few nanometers and thus much smaller than the minimum dimension of our nanostructures. As coherent effects in crystalline materials have been observed experimentally at low T (several K), we believe that additional study in the low temperature regime is warranted[40,45].

Finally, we did not observe a statistically significant effect of nanostructure orientation on κ_{eff} in SiN_x PNCs, unlike what had been documented in similar studies in crystalline Si. This difference indicated that, in amorphous materials, propagons are less likely to travel in straight lines compared to phonons in crystalline materials due to the disordered atomic lattice.

The small *p* and *n* inherent in BCP-templated nanostructures are ideal for scattering a significant portion of the phonon spectrum, making it possible to fabricate ultra-low thermal conductivity, precisely nanostructured membranes with useful, device-relevant thermal properties. Here, the results demonstrated that BCP DSA lithography techniques could be successfully applied to the field of PNC engineering as a viable way to overcome the resolution limit of top-down lithography techniques, enabling the design of high-precision experiments on phonon transport at length scales that were previously inaccessible. Our robust fabrication method could enable future studies to experimentally and theoretically probe the length scales of nanoscale phonon transport and phonon behavior over a range of temperatures, in both amorphous and crystalline materials.

2.6 References

1. Zhou, C. *et al.* Cite This: ACS Nano 2020, 14, 6980−6989 ACS Nano 2020, 14, 6980−6989 Downloaded via UNIV OF CHICAGO on. (2020). doi:10.1021/acsnano.0c01463

2. Tambo, N. *et al.* Ultimate suppression of thermal transport in amorphous silicon nitride by phononic nanostructure. *Sci. Adv.* **6**, eabc0075 (2020).

3. Wingert, M. C., Zheng, J., Kwon, S. & Chen, R. Thermal transport in amorphous materials: A review. *Semiconductor Science and Technology* **31**, 113003 (2016).

4. Schierning, G. Silicon nanostructures for thermoelectric devices: A review of the current state of the art. *Phys. status solidi* **211**, 1235–1249 (2014).

5. Maldovan, M. Sound and heat revolutions in phononics. *Nature* **503**, (2013).

6. Heremans, J. P., Dresselhaus, M. S., Bell, L. E. & Morelli, D. T. When thermoelectrics reached the nanoscale. *Nature Nanotechnology* **8**, 471–473 (2013).

7. Radziemska, E. Thermal performance of Si and GaAs based solar cells and modules: A review. *Progress in Energy and Combustion Science* **29**, 407–424 (2003).

8. Goodson, K. E., Flik, M. I., Su, L. T. & Antoniadis, D. A. Prediction and measurement of the thermal conductivity of amorphous dielectric layers. *J. Heat Transfer* **116**, 317–324 (1994).

9. Kaloyeros, A. E., Jové, F. A., Goff, J. & Arkles, B. Review—Silicon Nitride and Silicon Nitride-Rich Thin Film Technologies: Trends in Deposition Techniques and Related Applications. *ECS J. Solid State Sci. Technol.* **6**, P691–P714 (2017).

10. Chen, R. *et al.* Thermal Conductance of Thin Silicon Nanowires. *Phys. Rev. Lett.* **101**, 105501 (2008).

11. Hochbaum, A. I. *et al.* Enhanced thermoelectric performance of rough silicon nanowires. *Nature* **451**, 163–167 (2008).

12. Luckyanova, M. N. *et al.* Coherent phonon heat conduction in superlattices. *Science (80-.).* **338**, 936–939 (2012).

13. Ravichandran, J. *et al.* Crossover from incoherent to coherent phonon scattering in epitaxial oxide superlattices. *Nat. Mater.* **13**, 168–172 (2014).

14. Tang, J. *et al.* Holey silicon as an efficient thermoelectric material. *Nano Lett.* **10**, 4279–4283 (2010).

15. Yu, J.-K., Mitrovic, S., Tham, D., Varghese, J. & Heath, J. R. Reduction of thermal conductivity in phononic nanomesh structures. *Nat. Nanotechnol.* | **5**, (2010).

16. Nomura, M. *et al.* Impeded thermal transport in Si multiscale hierarchical architectures with phononic crystal nanostructures. *Phys. Rev. B - Condens. Matter Mater. Phys.* **91**, 205422 (2015).

17. Hur, K., Hennig, R. G. & Wiesner, U. Exploring Periodic Bicontinuous Cubic Network Structures with Complete Phononic Bandgaps. *J. Phys. Chem. C* **121**, 22347–22352 (2017).

18. Cahill, D. G. *et al.* Nanoscale thermal transport. *Journal of Applied Physics* **93**, 793–818 (2003).

19. Cahill, D. G. *et al.* Nanoscale thermal transport. II. 2003-2012. *Applied Physics Reviews* **1**, 11305 (2014).

20. Cahill, D. G., Watson, S. K. & Pohl, R. O. Lower limit to the thermal conductivity of disordered crystals. *Phys. Rev. B* **46**, 6131–6140 (1992).

21. Einstein, A. Elementare Betrachtungen über die thermische Molekularbewegung in festen Körpern. *Ann. Phys.* **340**, 679–694 (1911).

22. Slack, G. A. The Thermal Conductivity of Nonmetallic Crystals. *Solid State Phys. - Adv. Res. Appl.* **34**, 1–71 (1979).

23. Feldman, J. L., Kluge, M. D., Allen, P. B. & Wooten, F. Thermal conductivity and localization in glasses: Numerical study of a model of amorphous silicon. *Phys. Rev. B* **48**, 12589–12602 (1993).

24. Allen, P. B. & Feldman, J. L. Thermal conductivity of disordered harmonic solids. *Phys. Rev. B* **48**, 12581–12588 (1993).

25. Allen, P. B., Feldman, J. L., Fabian, J. & Wooten, F. Diffusons, locons and propagons: Character of atomie yibrations in amorphous Si. *Philos. Mag. B Phys. Condens. Matter; Stat. Mech. Electron. Opt. Magn. Prop.* **79**, 1715–1731 (1999).

26. Larkin, J. M. & McGaughey, A. J. H. Thermal conductivity accumulation in amorphous silica and amorphous silicon. *Phys. Rev. B - Condens. Matter Mater. Phys.* **89**, 144303 (2014).

27. Zhou, Y. & Hu, M. Record Low Thermal Conductivity of Polycrystalline Si Nanowire: Breaking the Casimir Limit by Severe Suppression of Propagons. *Nano Lett.* **16**, 6178–6187 (2016).

28. Zhan, T. *et al.* Phonons with long mean free paths in a-Si and a-Ge. *Appl. Phys. Lett.* **104**, 071911 (2014).

29. Braun, J. L. *et al.* Size effects on the thermal conductivity of amorphous silicon thin films. *Phys. Rev. B* **93**, 140201 (2016).

30. Sultan, R. *et al.* Heat transport by long mean free path vibrations in amorphous silicon nitride near room temperature. *Phys. Rev. B - Condens. Matter Mater. Phys.* **87**, 214305 (2013).

31. Kwon, S., Zheng, J., Wingert, M. C., Cui, S. & Chen, R. Unusually High and Anisotropic Thermal Conductivity in Amorphous Silicon Nanostructures. *ACS Nano* **11**, 2470–2476 (2017).

32. Yang, L. *et al.* Ballistic Phonon Penetration Depth in Amorphous Silicon Dioxide. *Nano Lett.* **17**, 7218–7225 (2017).

33. Graczykowski, B. *et al.* Thermal conductivity and air-mediated losses in periodic porous silicon membranes at high temperatures. *Nat. Commun.* **8**, 1–9 (2017).

34. Lee, J., Lim, J. & Yang, P. Ballistic Phonon Transport in Holey Silicon. *Nano Lett* **15**, 48 (2015).

35. Anufriev, R., Ramiere, A., Maire, J. & Nomura, M. Heat guiding and focusing using ballistic phonon transport in phononic nanostructures. *Nat. Commun.* **8**, 1–8 (2017).

36. Nomura, M. *et al.* Thermal phonon transport in silicon nanowires and two-dimensional phononic crystal nanostructures. *Appl. Phys. Lett.* **106**, 143102 (2015).

37. Sultan, R., Avery, A. D., Stiehl, G. & Zink, B. L. Thermal conductivity of micromachined low-stress silicon-nitride beams from 77 to 325 K. *J. Appl. Phys.* **105**, 043501 (2009).

38. Zink, B. L. & Hellman, F. Specific heat and thermal conductivity of low-stress amorphous Si-N membranes. *Solid State Commun.* **129**, 199–204 (2004).

39. Ftouni, H. *et al.* Thermal conductivity of silicon nitride membranes is not sensitive to stress The thermal conductivity of silicon nitride membranes is not sensitive to stress. *Phys. Rev. B Condens. Matter Mater. Phys.* 92 (2015). doi:10.1103/Phys

40. Maire, J. *et al. Heat conduction tuning using the wave nature of phonons*.

41. Segalman, R. A. Patterning with block copolymer thin films. *Materials Science and Engineering R: Reports* **48**, 191–226 (2005).

42. Lim, J. *et al.* Simultaneous thermoelectric property measurement and incoherent phonon transport in holey silicon. *ACS Nano* **10**, 124–132 (2016).

43. Anufriev, R., Maire, J. & Nomura, M. Reduction of thermal conductivity by surface scattering of phonons in periodic silicon nanostructures. *Phys. Rev. B* **93**, 45411 (2016).

44. Maire, J., Anufriev, R. & Nomura, M. Ballistic thermal transport in silicon nanowires. *Sci. Rep.* **7**, 1–8 (2017).

45. Koblinger, O. *et al.* Phonon stop bands in amorphous superlattices. *Phys. Rev. B* **35**, 9372–9375 (1987).

Chapter 3: Fabrication and characterization of polysilicon suspended membranes that functioned as phononic crystals and IR sensors with nanostructures templated by block copolymer cylinder self-assembly

Abstract

Introducing a periodic nanostructure into semiconductor materials has been shown to significantly lower the thermal conductivity by promoting phonon scattering. These nanostructured devices are broadly called phononic crystals (PnCs). PnC nanostructures have enormous potential to reduce the thermal conductivity of monolithic Si-based IR sensors, which lack the boundary resistance found in composite sensors but have a large native thermal conductivity. To test whether Si PnCs can improve IR sensitivity, polysilicon bolometric IR suspended membrane devices were designed and fabricated, and the thermal conductivity and IR sensitivity were measured. The PnC nanostructured devices were shown to have significantly reduced the thermal conductivity and an IR sensitivity enhancement of 2.5x relative to control (without nanostructure) devices. In addition to the design, fabrication, and measurements of these devices, we also present information about processing challenges and resolutions that were developed over the course of this work, which enabled significant improvements of the fabrication process the future experiments.

3.1 Introduction

Advances in lithographic technology over the past few decades have enabled fabrication of micro- and nanoscale devices, which has revolutionized the design, function, and performance of electronic devices[1,2]. Device sizes in conventional semiconductor chips are now small enough to be comparable to the mean free paths (MFPs) of thermal phonons in these materials. It is well documented that the thermal characteristics of a device (and by extension, performance) depend both on the critical dimensions as well as the intrinsic material properties[3,4,5,6]. Nanoscale thermal management is emerging as a critical area of device research, as it is relatively poorly understood

but intimately connected to performance of electronic devices. Thermal management is *especially* important for thermoelectric devices and IR sensors, which require both thermal isolation and low thermal conductivity (κ) in order for optimal performance. It is a significant materials engineering challenge to design high efficiency IR devices from conventional semiconductor materials because the thermal and electronic properties of a material are typically intensive and thus not customizable. Silicon is a highly desirable material for IR and thermoelectric applications because its electronic properties are highly customizable via doping. Si is also widely used in nanofabrication and readily fabricated into monolithic devices that lack contact resistance issues that arise in composite devices that degrade electronic performance. However, the thermal conductivity of Si is very large, which degrades the efficiency of Si-based devices.

Recently, introducing a periodic nanostructure into Si to form a phononic crystal (PnC) has emerged as a potential means of reducing the thermal conductivity of Si while preserving its mechanical and electronic properties. Conventionally, PnCs consist of a material into which a periodic array of holes is introduced. Fabrication schemes for Si PnCs with significantly reduced κ have been reported recently. PnC devices encompassing a variety of lattice types (square, hexagonal, etc.), pitches $\underline{p}$ (center-center spacing of the holes), and nanostructure porosities P, with minimum dimensions ranging from micrometers to a few tens of nanometers, have all been demonstrated to significantly lower κ[1,7–11]. The mechanism behind κ reduction in Si nanostructures beyond what is expected simply as a function of volume reduction has been attributed to a number of potential phenomena, with phonon scattering at interfaces being most popular explanation for uncooled devices.

Thermal phonons are thought to scatter from nanostructures that are comparable in size to or smaller than the average mean free path (MFP) (~300 nm in bulk Si). While lithographic

advances have made patterning at the sub-micron and sub-100 nm length scales possible, a number of challenges exist in fabricating nanostructures with minimum dimensions below ~60-80 nm. Phonons relevant to thermal conduction have MFPs that extend from 1-1000 nm; thus, the smaller the features of a nanostructure are, the more of the phonon spectrum it could theoretically scatter.

A method to significantly reduce κ is necessary for Si-based IR sensing devices to perform at a technologically useful level. Block-copolymer (BCP) nanolithography has emerged as a robust platform for templating inorganic nanostructures across a wide range of device applications[2,12]. Typically, the length scales attainable by BCP lithography range from $20 < p < 50$ nm, which is much smaller than the resolution limit of modern lithographic equipment. Thin film BCPs spontaneously self-assemble into highly uniform, polycrystalline nanostructures over large areas with very few process steps. BCP thin films are also easily integrated into standard lithographic processes, making BCP nanolithography an attractive way to fabricate ultrafine nanostructures like PnCs.

In this work, we present the fabrication and measurement of a prototype thermopile IR sensor from polysilicon-on-insulator substrates. IR sensitivity and thermal dissipation times for the porous PnC nanostructures were measured and compared to control devices that lacked nanostructuring. The nanostructured devices were found to have significantly reduced κ an IR sensitivity enhancement of 2.5 x relative to the control devices, indicating that the nanostructure behaved as a PnC and successfully manipulated the thermal properties of the pSi. Additionally, we describe a number of processing challenges that arose during the design and fabrication of these prototypes, which enabled us to significantly improve the design for the devices described in Chapter 5.

3.2 Experiment

3.2.1 Materials

Polysilicon-on-insulator substrates (pSi) were purchased from Electronics and Materials Corporation Limited with the following specifications: pSi (pSi), 100 nm; buried oxide (BOX), 2 μm; handle wafer, 535 μm; wafer diameter, 100 mm. Wafers were used without further cleaning. Acetone (≥ 99.5%), isopropyl alcohol (IPA, (≥ 99.9%), n-methyl pryrrolidinone (NMP, ≥ 99.0%), toluene (≥ 99.5%), and n-amyl acetate (≥ 99.0%) were purchased from Sigma Aldrich and used as received. For general photolithography, AZ MiR703 positive photoresist (PR703), AZ MiR1518 photoresist (PR1518), AZ MIF300 developer, and hexamethyldisilazane (HMDS) were purchased from AZ Materials. House deionized water (DI H_2O) was provided by the Pritzker Nanofabrication Facility. Piranha etch was made from conc. H_2SO_4 and 30% H_2O_2, which were purchased from Sigma Aldrich.

The BCP was a cylinder-forming polystyrene-block-poly(methyl methacrylate) (M_n 20k-b-50k, denoted as C2050, bulk period p = 37.5 nm) that was purchased from Polymer Source and used as-received. For perpendicular BCP assembly, wafers were first coated with a random poly(styrene-r-(methyl methacrylate)) copolymer (P(S-r-MMA)) mat that was designed to be energetically neutral to both blocks of the PS-b-PMMA. Solutions of all polymers used in this work were filtered prior to spin-coating using a 1 mL polypropylene syringe and an mdi Membrane Technologies PTFE syringe filter with 0.2 μm pore size. All polymer solutions were prepared in toluene.

3.2.2 Sample preparation

Full fabrication was completed on 100 mm wafers. Prior to thermal and IR measurements, the pSi wafer was cleaved into 1 x 1 cm^2 chips. The lithographic patterns were aligned to the

<100> direction of the Si handle wafer to enable easy cleaving. A number of different membrane device designs were present on each wafer.

First, four sets of cross-shaped alignment markers (100 μm long × 40 μm wide) alignment marks were etched 100 mm deep into the pSi/SiO_2 layers for photolithography. A Heidelberg MLA direct-write lithography system was used to pattern the alignment marks, and a PlasmaTherm Reactive Ion Etcher (RIE) with fluorine (F) chemistry was used to etch and complete the alignment mark formation.

The next step was ion implantation, which allowed the devices to function as IR sensors by modifying the donor density and compensation ratio[13]. Both doped and control (undoped) membranes were prepared. For each doped device, one leg was p-doped and the other n-doped. The rest of the wafer remained undoped. Lithographic masking was used to accomplish this selective doping. Liquid HMDS was spin-coated first to promote PR adhesion. PR1518 was spin-coated to a thickness of 2 μm, thick enough to prevent dopant penetration to the underlying substrate. First, the regions for p-doping were lithographically defined with a Heidelberg MLA Lithographer and developed with MIF300. The pattern was lightly O_2 plasma etched to remove any organic residue. The wafers were then shipped to Cutting Edge Ions, LLC for boron implantation at an energy of 10 keV and dose of 1.70×10^{15} ions/cm^2. The wafers were then shipped back, cleaned, re-patterned with areas for n-doping, which did not overlap the areas that had been p-doped, and shipped back to Cutting Edge Ions, LLC for phosphorous implantation at an energy of 30 keV and dose of 2.30×10^{15} ions/cm^2.

After each implantation step, the wafers were rigorously cleaned for 1 h with 130 °C piranha etch to remove all traces of ion-impregnated PR, which was difficult to remove. After piranha etching, wafers were thoroughly rinsed with DI H_2O and N_2 dried. Then, the dopants were

activated by annealing in a Solaris Rapid Thermal Annealer in an argon environment. The RTA treatment consisted of a ramp from room temperature to 1000 °C at a rate of 100 °C/min, a hold at 1000 °C for 10 minutes, and then ambient cooling. The target penetration depth for dopant activation was 100 nm. There was no overlap between the p- and n- doped regions after annealing, as they were separated by at least 500 nm in all designs.

Next, a PlasmaTherm Plasma-Enhanced Chemical Vapor Deposition (PECVD) tool was used to deposit a 50 nm of SiO_2 hard mask. SiO_2 was selected as the hard mask material due to its orthogonal etch chemistry with Si[14]. Then, the wafer was coated with the 57S mat, which was designed to be energetically neutral to both blocks of C2050. To prepare the mat, a 0.3 wt% solution of 57S in toluene was spin-coated to a thickness of ~9.5 nm. The mat was cross-linked by annealing on a hot plate in a N_2 glove box for 15 min at 220 °C. Then, excess unreacted mat was removed by ultrasonication in toluene for 5 min. After annealing and rinsing, the neutral mat thickness decreased slightly to 8 nm.

To fabricate SA structures, a 2 wt% solution of C2050 in toluene was spin-coated directly onto the 57S mat with a film thickness of 85 nm. Next, the wafer was annealed at 270 °C for 2.5 h on a hot plate in a N2 glove box. After 2.5 h, the wafer was thermally quenched on a metal block.

Sequential infiltration synthesis (SIS) was performed with an atomic layer deposition (ALD) tool to selectively infiltrate the PMMA block with vapor-phase precursors (trimethyl aluminum and DI H_2O) and nucleate a significant amount of AlO_x within the PMMA domain[15]. This resulted in a hybrid organic/inorganic PMMA/AlO_x film containing PS cylinders, which we refer to as the SIS-PS structure. This process was reported previously by our group for C2050 and is described in additional detail in Chapters 1 and 5[7,16,8].

After SIS, a 5 minute O_2 plasma etch was used to remove the PS cylinders from the SIS-PS structure, resulting in a nanoporous AlO_x SIS structure covering the entire 100 mm wafer. Next, a F-chemistry plasma etch was used to pattern transfer the holes from the SIS structure into the underlying SiO_2 hard mask across the entire wafer. The SIS structure was then removed by ultrasonication in MIF300 for ~2 minutes, after which the sample was cleaned by rinsing with IPA, acetone, and DI H_2O.

Next, lithography was used to define specific regions for pattern transfer into the underlying pSi. The areas for hole etching into pSi overlapped the p- and n-doped areas. HMDS was spin-coated onto the wafer to promote PR adhesion. PR703 was spin-coated to a thickness of ~1 µm directly on top of the Au layer, then soft-baked for 1 min at 95 °C. A Heidelberg MLA Lithographer was then used to define areas where hole etching would occur, which were then developed for 1 min in MIF300 developer. The size of this area varied between different membrane designs, but was consistently on the order of ~100-200 μm^2.

Next, RIE was used to etch transfer holes from the SiO_2 hard mask completely through the underlying pSi (exposing the underlying SiO_2 buried oxide at the base of each hole). A downstream asher was used to O_2 plasma etch the wafer to remove any crust from the PR. Then the PR was stripped by soaking in NMP at 80 °C for at least 1 h, followed by ultrasonication in NMP and IPA.

Lithography was then used to define the membrane shapes. The wafer was spin-coated with HMDS then coated with PR703 and soft-baked at 95 °C for 1 min. For rectangular membranes, a pair of rectangles was exposed in the location of each device, defining between them a rectangular region that varied in size on the order of ~100 μm^2, depending on the design (see Figure 3.3). The lithographic pattern was developed for 1 min in AZ MIF300 developer, then

lightly etched for 1 min in O_2 plasma to remove any residue from the pattern area. Next, Cl_2 plasma was used to etch completely through the pSi to expose the SiO_2 layer. After the pSi etch, a 3 min 70 °C O_2 etch was used to remove PR crust. Then, the PR was stripped by ultrasonication in 80 °C NMP, and the wafer was cleaned with NMP, acetone, IPA, and DI H_2O.

Next, lithography was used to define regions for aluminum deposition. The wafer was spin-coated with HMDS, coated with PR703, and soft-baked at 95 °C for 1 min. The Al pattern was then exposed by the Heidelberg and the pattern was developed in MIF300. A light O_2 plasma etch for 1 min was done to remove organic residue from the pattern area prior to Al evaporation. Then, a F-chemistry plasma etch was done to remove the SiO_2 hard mask from the pattern area. Next, 100 nm of Al was deposited using an Angstrom EvoVac e-beam evaporator at a rate of 2 Å/s. The wafer was then ultrasonicated in 80 °C NMP for 30-45 minutes to perform liftoff. Post-liftoff, the wafer was cleaned by ultrasonication in NMP, acetone, IPA, and then DI H_2O for 5 minutes each before N_2 drying. Finally, a 3 min 70 °C O_2 plasma etch was done to ensure no organic residue remained on the surface. At this point, the lithographic portion of the fabrication was complete.

Finally, a Memsstar VHF Etcher was used to perform a vapor-phase HF (VHF) etch, which selectively dissolved the underlying SiO_2 and suspended the membranes from the base substrate. The wafer was subjected to 1800 s of continuous HF vapor. At this point, a variety of measurement-ready membrane devices with an Al pad in the middle were completely fabricated and suspended from the base substrate.

3.2.3 Characterization

In-plane defectivity was assessed via top-down SEM (Carl Zeiss Merlin FE-SEM), while out-of-plane defectivity was inferred from etch-transfer tests into the pSi. For select membrane designs, both the thermal dissipation and IR sensitivity were measured.

Thermal dissipation was measured via Time Domain Thermoreflectance (TDTR). Our TDTR system used two laser diodes (LDs) with wavelengths of 785 and 852 nm. The 852 nm wavelength LD, the pump beam, was electrically modulated to create a quasi-continuous wave with a duration of 4 μs and pulsed every 60 ms to allow for thermal equilibration between pulses (Cite Naoki's paper). The pump beam was used to heat the central Al pad on each device. The 785 nm wavelength LD, the probe beam, was operated in a continuous wave to measure the changes in reflectivity (ΔR) of the central Al pad as its temperature changed. The pump and probe beams were each coupled to a separate optical fiber, which were then attached to a fiber combiner with a single fiber output, and were then perfectly aligned by a collimator before irradiating the sample. The merged pump/probe beam was focused onto the central Al pad of each nanoporous Si device. The spot size of the combined beams was fixed at ~6 μm using an objective lens at 10x magnification, and the beam position was adjusted by monitoring the reflected beam profile using an infrared viewer. The power of the pump and probe beams were set at 50 μW and 1 mW, respectively, to ensure the temperature change (ΔT) of the Al pad remained lower than 10 K. A balance photo-detector coupled with a digital oscilloscope was used to measure the power of the probe beam reflected by the Al pad. Each sample was measured 3 times and 4 identical devices per condition were measured for a total of 12 measurements per sample condition. All measurements were carried out at room temperature, and the standard error for each measurement was less than 3 %. The method used for standard error computation is described in Chapter 5.

IR sensitivity of select membranes was determined by measuring the thermoelectromotive voltage against irradiated optical laser power. Measurements were conducted in a vacuum chamber at 0.5 Pa of pressure. An optical laser with a wavelength of 1550 nm was used to irradiate the Al pads in the center of the nanoporous membranes through the view port of the vacuum chamber. A signal amplifier (Model 5113 Pre-AMP, Signal Recovery) collected the reflected laser signal and transferred it to an oscilloscope (MSO56, Keithley). To obtain the thermoelectromotive voltage, the laser power was pulse modulated in 100 ms period. The gain of the signal amplifier was set to 5000, and laser power was adjusted from 0.1 to 3 mW. The raw signal from the oscilloscope was averaged 300 times to improve accuracy. The IR sensitivity was obtained by measuring the amplitude of detected sensor signal and dividing by the irradiated laser power.

3.3 Results

3.3.1 Device fabrication

First, p- and n-doped regions were created via selective dopant implantation enabled by lithographic PR patterns as illustrated in Figure 3.1. Each doped membrane had one p- and one n-doped leg each, as illustrated in Figure 3.1. There was optical contrast between the p- and n-doped regions after implantation. Then, the wafer was subjected to a high temperature rapid thermal annealing (RTA) process to activate the dopants to a depth of ~100 nm. The optical contrast disappeared post-RTA.

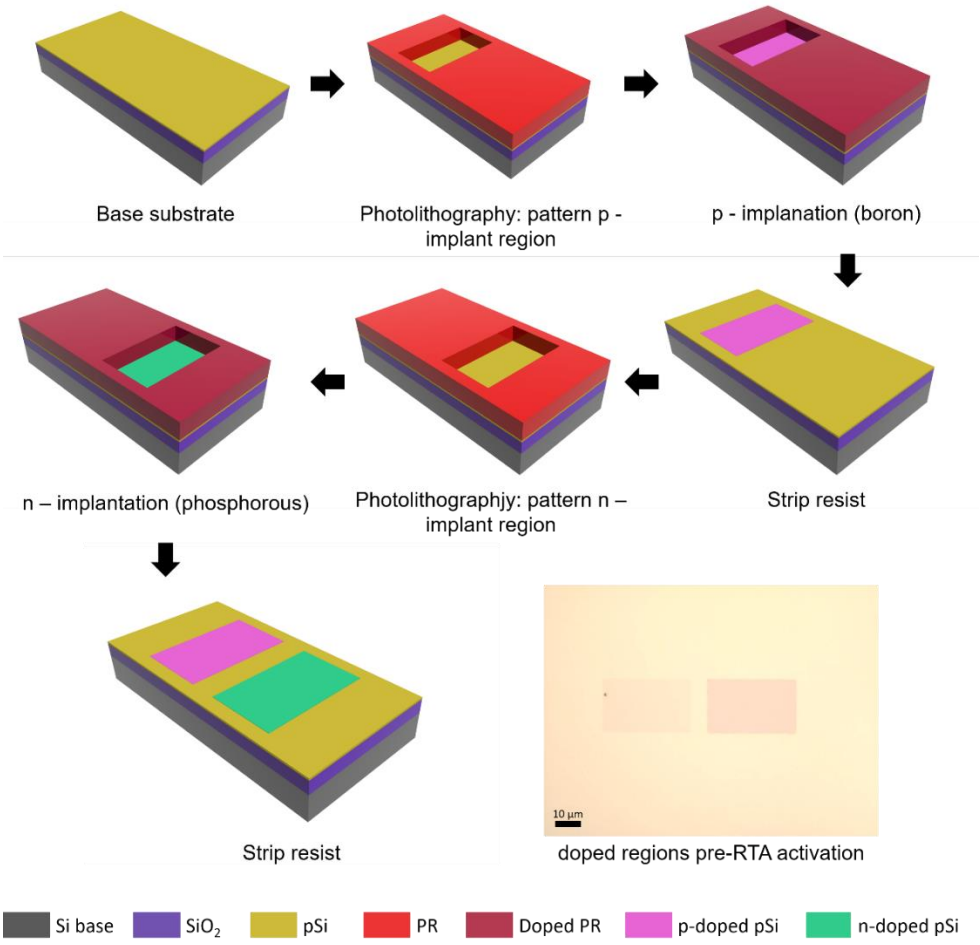


Figure 3.1 Illustration of the fabrication process for area-selective ion implantation for pSi suspended membranes. Wafers were lithographically patterned with regions for p-doping, then n-doping. After both B- and P- implantation were complete, the wafers were characterized in optical microscopy. An optical micrograph of the doped regions prior to ion activation is shown at the bottom right.

After dopant implantation and activation, the BCP layer was prepared and converted to an etching template via SIS, as illustrated in Figure 3.2. The SIS process converted the organic self-assembled nanostructure, which is of limited utility as an etch mask, into a mask with suitable etch contrast suitable for pattern transfer. Next, the PS domains were selectively removed from the SIS-PS structure with a light O_2 plasma etch. Then, RIE was used to transfer the holes into the SiO_2 hard mask. Due to slight process drift caused by the chemical environment inside the RIE,

the SiO_2 hard mask etch also slightly etched the underlying pSi, resulting in slight pitting across the surface. The SIS structure was then stripped in developer. Next, photolithography was used to define areas where hole etching into the pSi would occur, which overlapped with the P- and B-implanted areas. The hard mask was used as an etching template, and a Cl_2/O_2 plasma was used to etch-transfer the holes in the template completely through the underlying pSi. Then, the resist was stripped and the wafer was cleaned.

Next, photolithography was used to define the shape of the membranes by exposing two rectangular areas that defined between them the shape of the membrane. The pSi in these exposed areas was completely removed by Cl_2 plasma, exposing the SiO_2 BOX layer. Next, the membranes were prepped for TDTR measurements, which require Al pads. To form the Al pads, a lithographic pattern defining 3 pads per membrane was created. Then, a F-chemistry plasma etch was used to remove the SiO_2 hard mask from this pattern area. Next, 100 nm of aluminum was deposited via e-beam evaporation. Finally, a liftoff process was used to complete the Al pad formation, which resulted in three square pads per membrane, one in the center plus one pad at each end. No holes were present beneath the center pad.

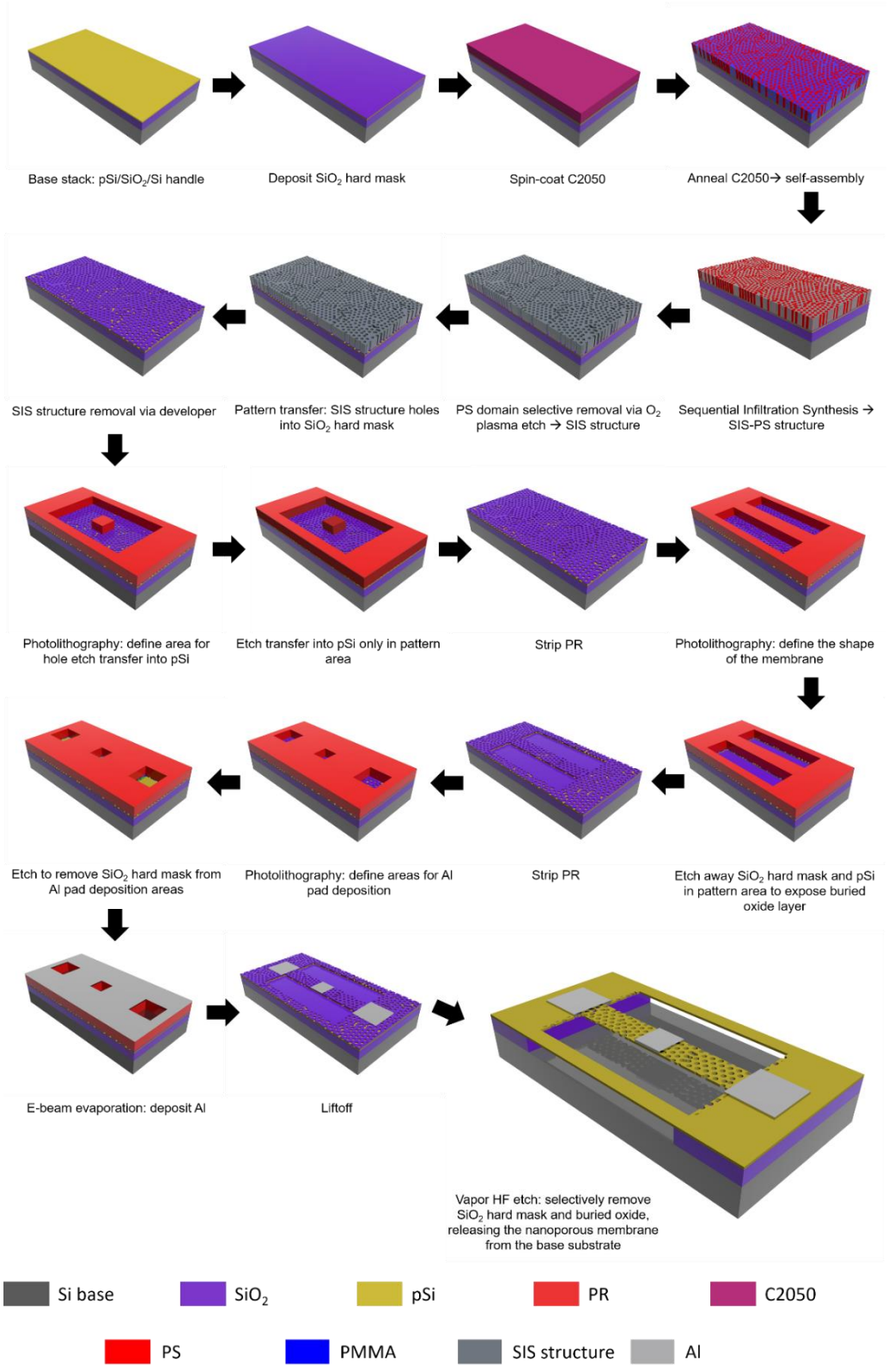


Figure 3.2 An illustration of the post-ion implantation process flow to fabricate nanostructured IR sensors from polysilicon-on-insulator wafers.

To suspend and thermally isolate the membranes from the base wafer, a VHF etch was used to selectively dissolve the underlying SiO_2 in areas where it had been exposed. This step also removed the remainder of the SiO_2 hard mask from the entire wafer. At this point, a variety of rectangular membranes completely fabricated and released from the base substrate, and were ready for measurement. While a hundreds of different membranes with different designs were fabricated, we will focus our discussion on two different membrane designs, called Sensor 1 (S1) and Sensor 2 (S2). The design file for S1 and S2 compared to the fabricated structures illustrated in Figure 3.3 All membrane designs and all membrane types were fabricated simultaneously on the same wafer. Both nanostructured (porous) and control (nonporous) versions of designs S1 and S2 will be discussed.

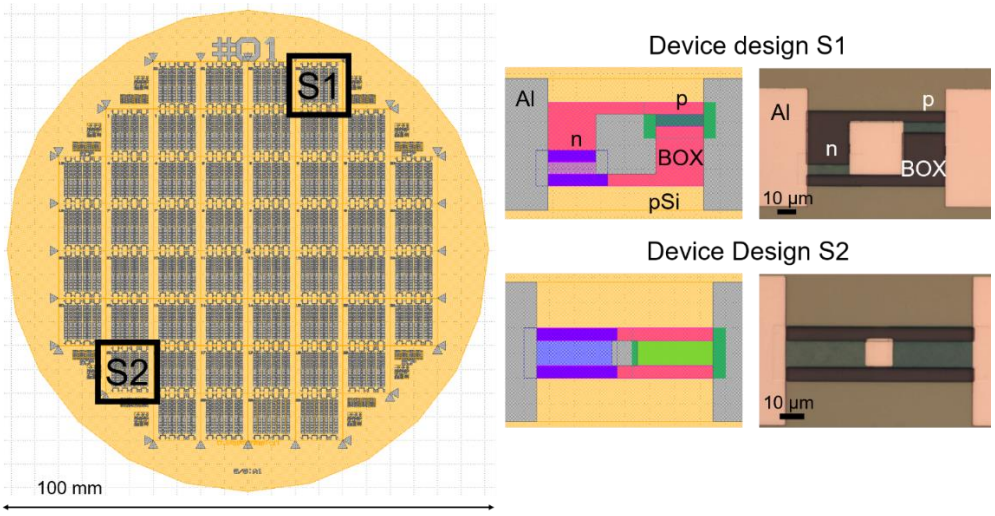


Figure 3.3 Images of different kinds of devices present on the full wafer design. On the left, the full 100 mm wafer design file is shown. The wafer is visibly divided into 52 1 × 1 cm^2 chips. Each 1 × 1 cm^2 chip contains an array of 32 identical membranes with the same design, doping, and porosity characteristics. To the right, optical micrographs are shown for S1 and S2 devices compared to their design files. The optical micrographs were taken prior to VHF etching, so the devices are not released from the base wafer in these images. The porous nanostructure causes a color change under optical inspection, so the membrane legs appear to be a different color (blue-brown) than the rest of the pSi (taupe).

3.3.2 Characterization

Samples were examined post-fabrication in top-down and tilt SEM (SU8220, Hitachi), while out-of-plane defectivity was inferred from etch-transfer tests into the Si (see section 3.6 for details).

The TDTR system thermal dissipation measurements used two laser diodes (LDs) with wavelengths of 785 and 852 nm. The 852 nm wavelength LD, the pump beam, was electrically modulated to create a quasi-continuous wave with a duration of 4 μs and pulsed every 60 ms to allow for thermal equilibration between pulses[7,8]. The pump beam was used to heat the central Al pad on each device. The 785 nm wavelength LD, the probe beam, was operated in a continuous wave to measure the changes in reflectivity (ΔR) of the central Al pad as its temperature changed. The pump and probe beams were each coupled to a separate optical fiber, which were then attached to a fiber combiner with a single fiber output, and were then perfectly aligned by a collimator before irradiating the sample. The merged pump/probe beam was focused onto the central Al pad of each nanoporous Si device. The spot size of the combined beams was fixed at ~6 μm using an objective lens at 10x magnification, and the beam position was adjusted by monitoring the reflected beam profile using an infrared viewer. The power of the pump and probe beams were set at 50 μW and 1 mW, respectively, to ensure the temperature change (ΔT) of the Al pad remained lower than 10 K. A balance photo-detector coupled with a digital oscilloscope was used to measure the power of the probe beam reflected by the Al pad. Each sample was measured 3 times and 4 identical samples per condition were measured for a total of 12 measurements per sample condition. All measurements were carried out at room temperature, and the standard error for each measurement was less than 3%. The method used for standard error computation is described in Chapter 5.

IR sensitivity of select membranes was determined by measuring the thermoelectromotive voltage against irradiated optical laser power. Measurements were conducted in a vacuum chamber at 0.5Pa of pressure to minimize convective heat loss and ensure that heat dissipated through the membrane only. The central Al pads were irradiated with an optical laser through the view port of the vacuum chamber. The laser signal was collected by a signal amplifier and transferred to an oscilloscope. The experimental setup is illustrated in Figure 3.4.

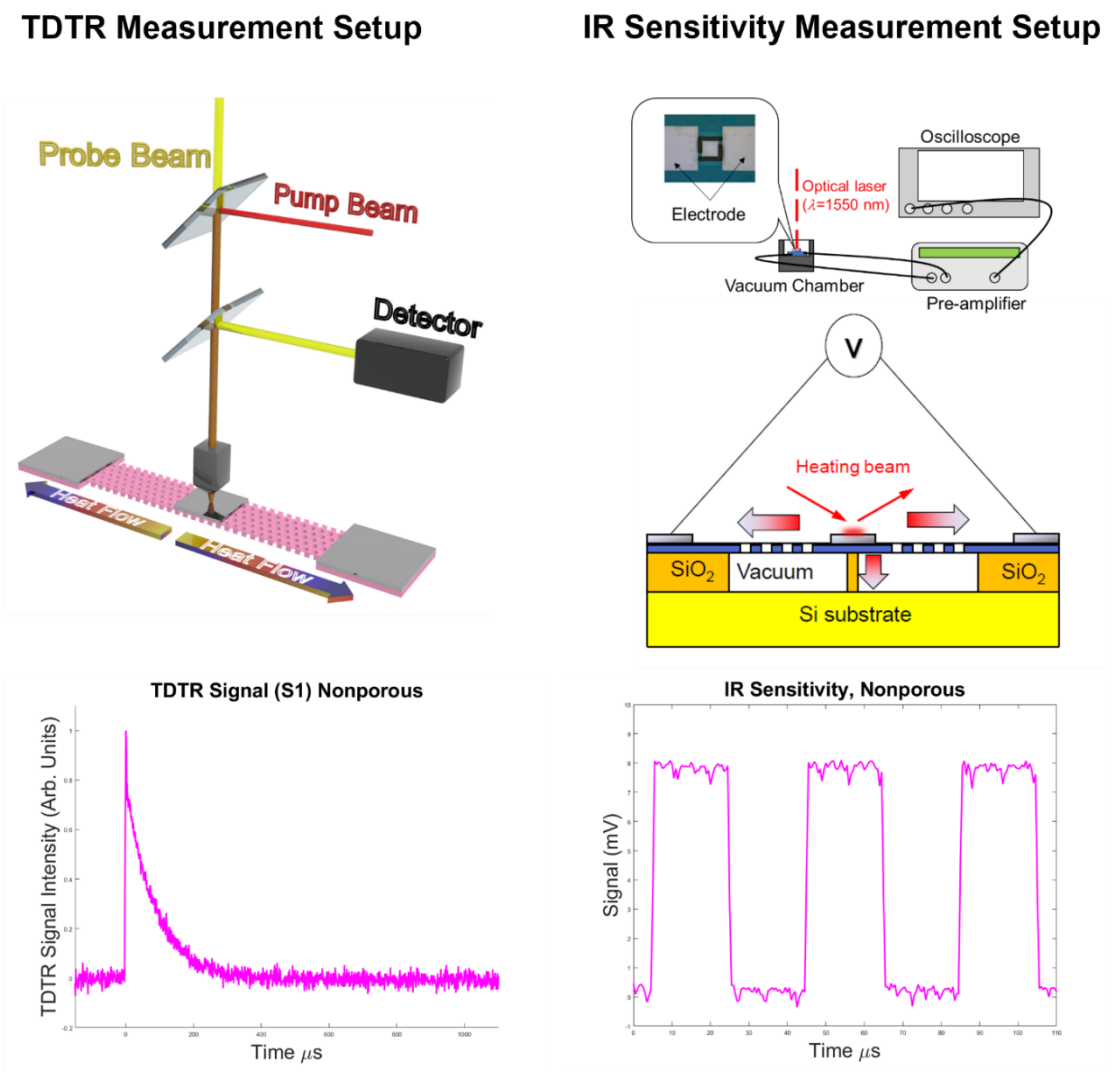


Figure 3.4 Thermoreflectance and IR sensitivity measurement setups. The TDTR setup is shown on the left, and the IR sensitivity measurement setup is shown on the right. Examples of the measurement signals for nonporous S1 devices are shown on the bottom. Details about the measurements are described in text.

The optical laser with 1550nm wavelength was irradiated onto the suspended absorber through the view port of vacuum chamber. In order to obtain the thermoelectromotive voltage, the laser power was pulse modulated in 100 ms period. Since the thermal decay time of fabricated sensor is much smaller than 1 ms, this was considered to be a steady state measurement. The gain of signal amplifier was set to 5000, and laser power was adjusted from 0.1 to 3 mW. The obtained sensor signal was plotted in figure 3.4. The raw signal from the oscilloscope was averaged 300 times to improve measurement accuracy. The sensor sensitivity was obtained by measuring the amplitude of detected sensor signal and dividing by the irradiated laser power.

3.4 Discussion

Detailed SEM micrographs of S1 and S2 devices are shown in Figure 5, including a magnified view of the porous nanostructure. While the nanostructure was highly defective as seen in Figure 5, the average dimensions were as follows: pitch p = 37.5 nm, pore radius r = 7.5 nm, neck width n = 23 nm, and porosity P = 14%. The defectivity of the nanostructure is addressed in more detail in Section 6.

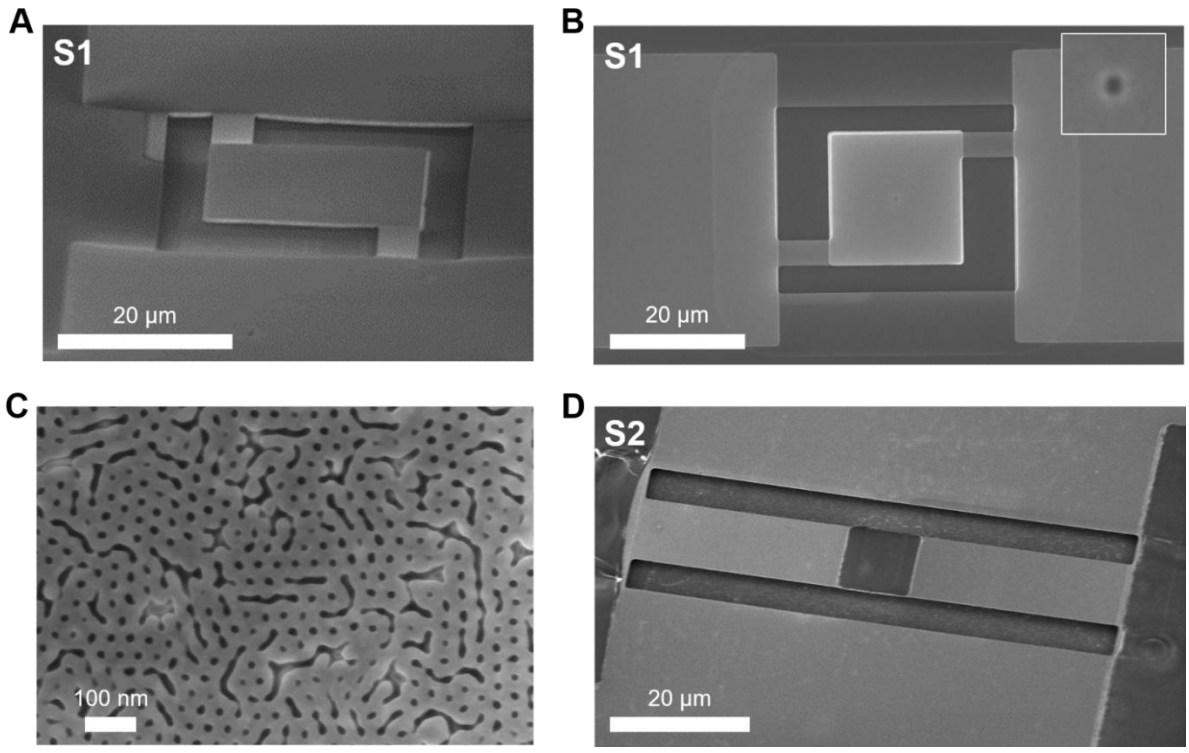
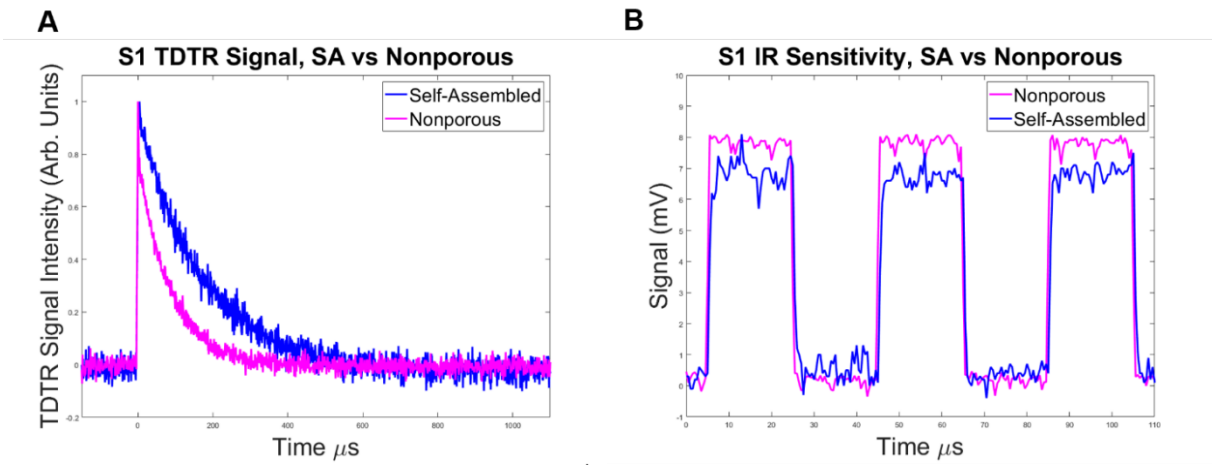


Figure 3.5 SEM micrographs of S1 and S2 devices, with top-down, tilt, and magnified views shown. (A) A tilt-view of a nanoporous S1 device showing it is not in contact with the base substrate. (B) A top-down view of a control S1 device. The dark spot in the center of the square is the SiO_2 support pillar, which is magnified in the inset. (C) A magnified view of the self-assembled BCP-templated nanostructure. (D) A low-angle tilt view of a nanoporous S2 device. The central square in A, B, and D is the Al pad for TDTR measurements. The two rectangular legs attached to the square are either nonporous (control) or nanoporous (PnC) regions.

Due to fabrication challenges, the membranes were supported by a small SiO_2 pillar below the central Al pad, rather than being fully released from the base substrate. This SiO_2 support pillar was formed by shortening the VHF etch, resulting in incomplete removal of the underlying SiO_2. The VHF etch works towards the center of the membrane from areas where SiO_2 was lithographically exposed (at the membrane edges and through the nanopores), so SiO_2 pillars were only left below the nonporous, central Al pad. The SiO_2 pillar is visible as a small dark spot in the center of the Al pad as shown in Figure 3.5B. While the SiO_2 pillar did degrade the device performance by providing thermal contact to the base substrate, the physical support was needed in order to measure these devices at all.



C

Design S1	Self-Assembled	Nonporous
τ (μs)	167	82.7
Irradiated Laser Power (mW)	1.3	3.4
Signal Amplitude (mV)	6.7	7.9
Sensitivity (V/W	5.2	2.3

Figure 3.6 TDTR (A) and IR sensitivity (B) measurements on Design 1 membranes with and without holes templated by BCP self-assembly (SA). Precise values for τ, irradiated laser power, signal amplitude, and IR sensitivity are listed in (C).

Measurement results for thermal conductivity and IR sensitivity for both designs are shown in Figure 3.6. Due to mechanical issues with S2, we will focus our discussion on measurement results from S1 devices only. Additional discussion on S2 device measurements is available in Section 3.6.5. For S1 devices, nonporous control and porous membranes templated with self-assembled (SA) BCP holes had thermal decay times τ of 83 μs and 170 μs, respectively. Due to the presence of the SiO_2 support pillar, deriving a precise value for thermal conductivity from τ is challenging. However, we can discuss the relative thermal conductivities by comparing the ratio of the self-assembled porous τ_{SA} to the nonporous, control τ_{np}. The τ extracted from the TDTR signal is a measure of the thermal resistance R and heat capacity C of the material ($\tau \propto CR$). Therefore, we can use the ratio of τ_{SA} to $\tau_{control}$ to compare the relative magnitude of R_{SA} to $R_{nonporous}$ in the following way,

$$\Delta R \equiv \frac{R_{SA}}{R_{nonporous}} = \frac{\tau_{SA}}{\tau_{nonporous}} \cdot \frac{1}{1-P} \tag{3.1}$$

where *P* denotes the porosity of nanoporous PnCs. We were thus able to calculate that the ratio of *R* between the control and porous S1 devices was 2.3, showing that heat dissipated much more slowly through the nanostructure than the control devices. Thus, the nanostructure successfully reduced the thermal conductivity of the device and functioned as a phononic crystal.

Next, we will discuss the IR sensitivity for porous and nonporous S1 devices. To ensure that the increase in temperature of the absorber (the central Al pad) due to laser irradiation was the same between the porous and nonporous membranes, laser power was adjusted until the signal voltage was similar for both devices. Then, the IR sensitivity of each device could be obtained by dividing the signal voltage by irradiated laser power. As shown in Figure 3.6, the IR sensitivity for nonporous and self-assembled devices were 2.3 V/W and 5.2 V/W, respectively. Thus, for the S1 devices, the IR sensitivity for the nanostructured device was enhanced 2.26 times relative to the control device. Thus, the phononic crystal was successfully able to improve the IR sensitivity of these devices.

In general, the sensitivity of an uncooled IR sensor is proportional to *R*. An IR sensor detects the temperature increase of absorber due to IR absorption, so maximizing the range for temperature increase results in higher sensitivity. In a vacuum environment, convective heat loss is minimized, and it can be assumed that the primary path of heat flow is through the suspended devices; thus, we can say that the IR sensitivity is proportional to *R*. From TDTR, we were able to calculate the ratio of *R* between the porous and nonporous devices was 2.3. This is consistent with IR sensitivity increase for the porous devices relative to the control devices. We believe that these results show that introducing a periodic nanostructure into an IR sensor device design measurably improves the sensitivity.

3.5 Conclusions

In summary, we successfully designed and fabricated suspended polysilicon membranes, with nanostructures templated by block copolymer nanolithography. The nanostructured devices significantly increased the thermal dissipation time and functioned as phononic crystals. The phononic crystal devices showed significant IR sensitivity enhancement despite a number of fabrication issues including small porosity, nanostructure defectivity, and mechanical issues that required SiO_2 support pillars, all of which degraded the device performance. Fabricating these sensors with larger porosity, fewer defects, and without the SiO_2 support pillars would likely result in a much larger *R* ratio and therefore a much larger IR sensitivity enhancement. Regardless, we believe our results support the hypothesis that controlling the propagation of heat through an IR sensor is essential for improving performance. Our results demonstrate that even a defective phononic crystal is capable of significantly improving the IR sensitivity in an IR sensor. Furthermore, we show that the thermal properties of Si can be engineered independently of the electronic properties by both doping and nanostructuring the Si. We show that BCP nanolithography is an excellent strategy for fabricating phononic crystals with dimensions small enough to reduce thermal phonon transport in Si.

3.6 Supplementary process information: challenges and solutions

Developing a new process flow to fabricate nanostructures is difficult and time consuming. It is equally challenging to take an existing process flow and modify it for another similar (but not identical) substrate. In our case, adapting an existing nanoporous membrane fabrication process from SiN_x (Chapter 2) to polysilicon-on-insulator was extremely challenging. In this supplementary section, the most significant challenges we encountered in adapting our process from SiN_x to pSi, as well as process improvements we made to overcome those challenges, are

described. The improved process was incorporated into the silicon-on-insulator fabrication work presented in Chapter 5.

3.6.1 BCP assembly and pattern transfer quality

The quality of the self-assembled C2050 nanostructure caused a number of complex problems in during pattern transfer into the pSi. Importantly, in this work a different neutral mat was used for perpendicular assembly than in the SiN_x work. The previous neutral mat was from a custom synthesized lot of PS-*r*-PMMA that was completely depleted by the time this work began. We attempted to synthesize an identical PS-*r*-PMMA neutral mat with for this work.

This new neutral mat affected the overall pattern transfer quality of the BCP holes into the pSi, as illustrated in Figure 3.7. In BCP films, defects are compositionally balanced. However, these defect structures are three dimensional in nature, meaning that the morphology visible at the top of the film is not necessarily indicative of the morphology at the bottom interface. This is especially true if the bottom interface is not perfectly energetically neutral both blocks. While the 3D through-film morphology of a nanodomain (a cylinder) is impossible to know without doing TEM tomography[17], we were able to infer the assembly quality of our films through etch transfer tests into the pSi. We found that when pattern transferring BCP features that were annealed on the new mat, long worm-like holes regularly appeared. These defects were especially concentrated at the grain boundaries as shown in Figure 3.7b. These wormlike defects were not visible by top-down imaging of the BCP prior to etching, which is the main reason we did not initially notice problems with the neutral mat until they came out later in processing.

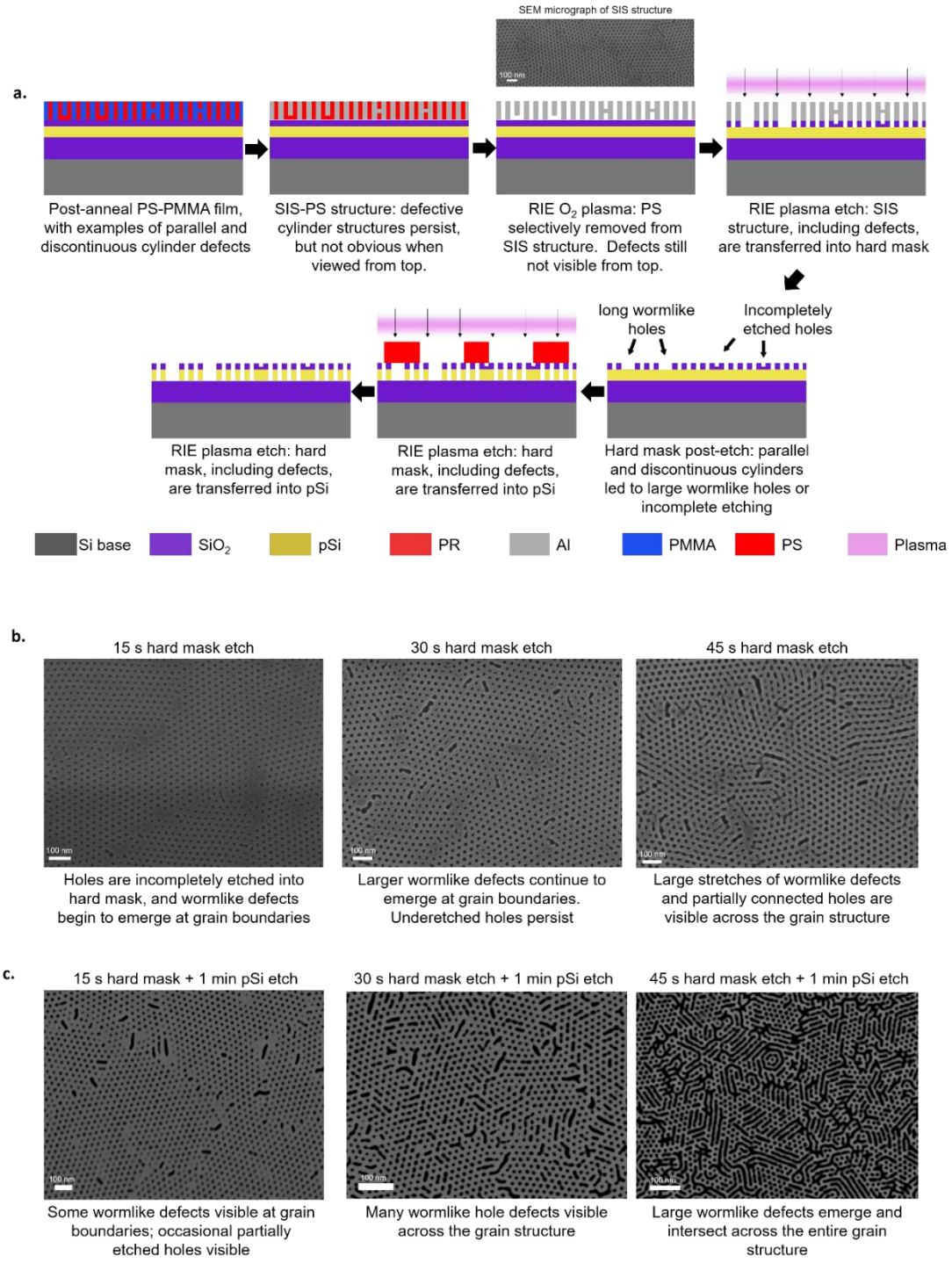


Figure 3.7 Schematic illustrations of the hypothesized mechanism by which large defect structures were etch transferred into pSi as a result of the imperfect 57S neutral mat base. In (a), defects in the annealed PS-PMMA film, including parallel PS cylinders at the bottom interface and discontinuous cylinders, led to the formation of a defective SIS structure. Note that the defects were not obvious from a top-down view, as shown in the SEM micrograph of the SIS structure in 6a. Defects in the SIS structure were transferred via a top-down plasma etch into the SiO_2 hard

Fig. 3.7, continued
mask, resulting into incompletely etched holes and large wormlike hole defects. These defects were then transferred into the pSi in subsequent etch steps, resulting in large defect concentrations in the pSi films. In (b-c), the approach we used to infer PS-PMMA and neutral mat film suitability for pattern transfer is shown. The image series shows three samples prepped with the 57S neutral mat and PS-PMMA film after pattern transfer into both (b) the hard mask and (c) the pSi (the entire process illustrated in (a)). As the etch time on the SiO_2 hard mask increases, many defects appear. The ~50 nm thick hard mask needed approximately 45s to be completely etched through, so the large defectivity significantly degraded the utility of our nanostructures.

We believe that the root cause of this problem was that the new lot of 57S neutral mat used in this work was not perfectly neutral to the C2050, resulting in occasional parallel cylinders on the bottom interface as illustrated in Figure 3.7a. The areas of the SIS template with a perpendicular cylinder sitting directly on top of a parallel cylinder had thinner AlO_x in the vertical direction than in areas with continuous cylinders. As a result, the etching process likely (1) completely etched through the perpendicular part of the template and exposed the parallel wormlike defects, etching those into the SiO_2 hard mask, or (2) collapsed the parts of the template with mixed morphology in the vertical direction, etching the collapsed wormlike defects into the SiO_2 hard mask. Any defects present in the hard mask were then subsequently pattern-transferred into the pSi. These are the most likely reasons for the presence of large, wormlike defects in our etched pSi nanostructures. These defects were undesirable for a number of reasons, and we believe that they compromised the structural integrity of the membranes and made them more prone to collapsing. In future work, we were able synthesize a new neutral mat (67% S) that eliminated all these issues.

3.6.2 Etching inconsistencies for 100 mm wafer due to BOX insulating layer

Another set of significant design challenges arose while adapting our membrane fabrication process from SiN_x to pSi due to the differences in the stacks and sample size. For the SiN_x work, the stack consisted of 70 nm Low Pressure Chemical Vapor Deposited (LPCVD) SiN_x on top of a

535 μm thick Si base wafer. For the pSi work, the stack consisted of 100 nm pSi on top of 2 μm of SiO_2 buried oxide (BOX), with both layers stacked on top of a 535 μm thick Si base wafer. The thick BOX layer, which was a necessary sacrificial layer, was very electrically insulating and led to difficulties with plasma etching the wafers.

In the SiN_x work, the nitride was directly in contact with the Si base wafer. Si has a large thermal conductivity, which even distribution of heating during dry etching. Our previous samples were also processed as ~40 mm^2 pieces cut from a 100 mm wafer and mounted on a carrier Si wafer. This resulted in uniform thermal and electrical contact between the sample carrier wafer, which led to consistent and uniform etching profiles. By contrast, the pSi samples were processed as 100 mm wafers, and were loaded directly into and clamped by the RIE tool. The tool detects a bias between the plasma and the clamp where the wafer is held. If electrical contact between the sample and the clamp is good, the etch proceeds normally. But, as was often the case with the pSi wafers, an insulating layer preventing electrical contact between the wafer and the clamp can cause the etch to short or produce non-uniform results. We frequently had trouble with our etches shorting or producing non-uniform results, and believe that the BOX layer prevented consistent thermal and electrical contact between the top surface and the clamp.

We were able to resolve these issues fully in future work by (1) cutting the pSi wafers into 20-45 mm^2 chips for processing and (2) using thermal tape to adhere the samples to carrier Si wafers during etching. These steps resulted in reproducible and high quality etching results on future SOI-based samples. For 100 mm wafers, we found that etching 4-6 ~20 μm^2 holes all the way through the BOX layer, then filling those holes with Au, provided the necessary electrical contact between the top and bottom layers of the stack for the RIE etches to proceed normally.

3.6.3 SiO_2 hard mask: use and removal complications

PS-b-PMMA is a challenging material to use directly as an etch mask due to its relatively low etch selectivity. Pattern transferring the polymer structure into a thin inorganic hard mask with high etch selectivity (like SiO_2) is a common intermediate step in pattern transfer. While our group had previous success in using hard masks for BCP pattern transfer, using a hard mask in this work ended up being extremely problematic because it was almost impossible to remove without damaging the pSi and/or BOX layers.

As illustrated in Figure 3.2, the hard mask was present on the wafer up until the final VHF step. SiO_2 was selected as the hard mask material for two reasons: (1) we had successful and established processes for it, and (2) it has orthogonal etch chemistry to Si. However, removing this hard mask turned out to be significantly more difficult here than in our previous work. The hard mask in the SiN_x work was removed by a buffered HF solution immediately after pattern transfer, which did not etch Si or SiN_x. However, a wet etch was not appropriate for removing the hard mask in the pSi stack due to the presence of the BOX layer. Using HF to remove the hard mask in this process would have resulted in the nanoporous areas of the wafer being prematurely released from the base wafer before fabrication was complete, rendering them useless. Because of this constraint, we elected to not remove the hard mask after pattern transfer.

Leaving the hard mask on the wafer resulted in additional difficulties during the Al pad deposition step, as illustrated in Figure 3.8. The Al pads could not be deposited directly atop the hard mask, because (1) they needed to be in thermal contact with the pSi, and (2) the SiO_2 would get dissolved during VHF etching and warp and disfigure the pads. As wet etching the hard mask was not an option, a F plasma etch was used to remove the hard mask from areas where Al would be deposited prior to deposition, as illustrated in Figure 3.8. However, the dry etch chemistry

between Si and SiO_2 is not completely orthogonal, and a small amount of overetch into the pSi occurred. The amount of overetch was difficult to control, and was typically 5-15% of the thickness of the pSi layer (5-15 nm). This resulted in (1) the Al pads being partially inset into the membrane and (2) partial removal of doped Si close to the surface. The first caused issues with the mechanical stability of the membranes, while the latter presented difficulties in evaluating the IR performance of the membranes.

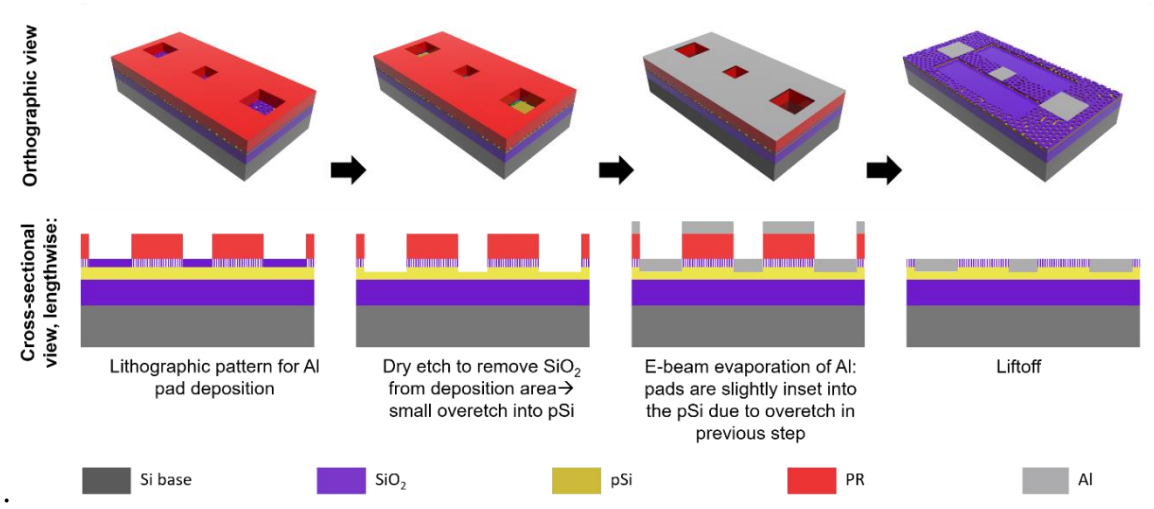


Figure 3.8 Illustration of processing challenges posed by removing the SiO_2 hard mask from below the Al pad deposition area prior to deposition. Dry etch chemistries are not completely orthogonal for Si and SiO_2. It was imperative for the function of the Al pads that no SiO_2 remained in the deposition area. Therefore, the layer had to be slightly overetched into the underlying pSi, typically on the order of 5-15 nm of pSi removed. This was significant, as the total thickness of the pSi layer was 100 nm. After Al evaporation and liftoff, the Al pads were slightly inset into the pSi layer. This likely caused some mechanical weakening of the membrane post-VHF etching to release from the base substrate.

The hard mask also affected the quality of the nonporous control membranes. A number of nonporous membranes were fabricated in addition to the porous membranes for control measurements. The BCP film preparation had to happen before any topography was introduced to the wafer surface (such as Al pads), which could cause spin-coating defects in the BCP film. Holes were first etch transferred into the hard mask across the entire wafer. After this, the SIS

structure was stripped, the areas for pattern transfer into the pSi were patterned, and the holes were selectively etched into pSi only in those areas. However, because the SiO_2 dry etch also slightly etched pSi, small dimples a few nanometers deep were etched into the pSi across the entire wafer, including areas that were meant to be nonporous as illustrated in Figure 3.9. This was an undesirable processing artefact because phonons are affected by surface roughness, so the dimpling skewed the control experiments.

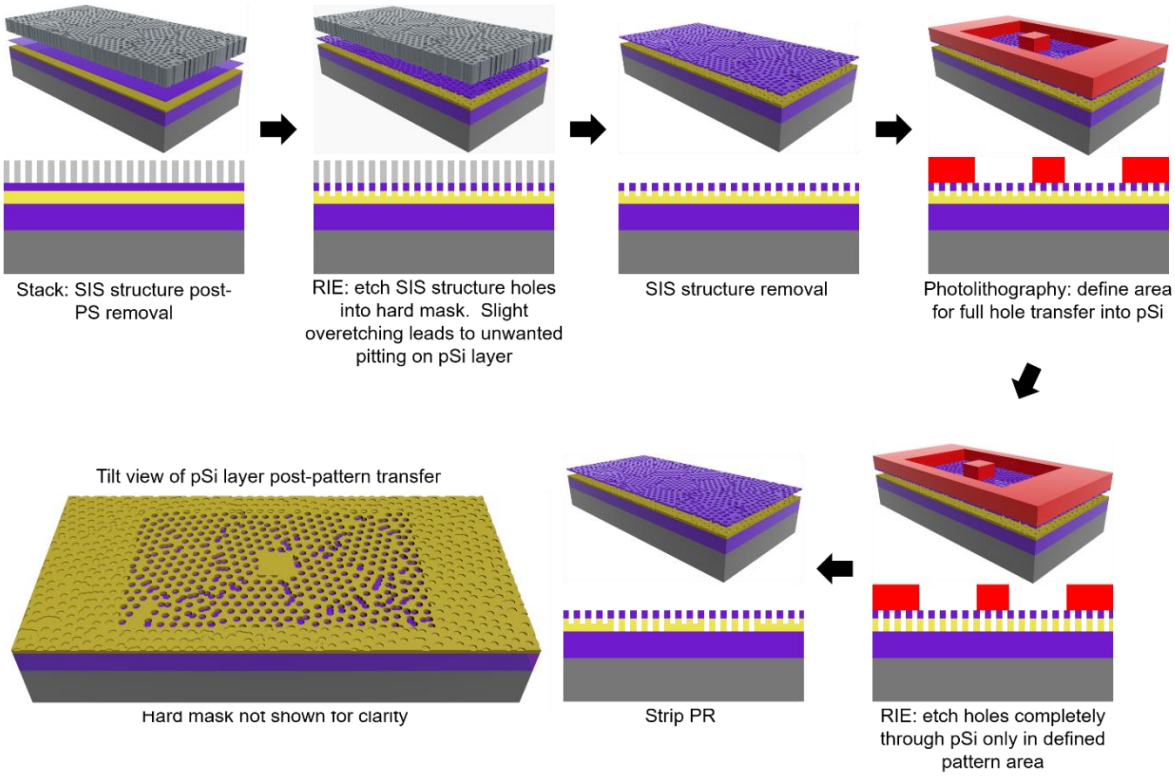


Figure 3.9 Process flow schematic depicting how the etch transfer process resulted in unwanted pitting in the pSi layer. The stack is expanded vertically to show effects on the pSi layer during processing. When the pattern transfer from the SIS structure into the hard mask occurred, a small amount of overetching resulted in light pitting in the pSi layer. This occurred across the entire wafer, both in areas where hole etching into the pSi was wanted and unwanted. The wafer was then lithographically patterned to define the area for hole transfer into the pSi, and the pSi was etched. After hole etching, the pSi layer had areas of complete hole etching where the pattern was defined, and regions of pitting outside the pattern area, as shown in the final graphic. The scale of the pitting is exaggerated in this schematic for illustrative purposes.

3.6.4 RTA damage during dopant activation

Dopant activation was also a problem in this process flow. After ion implantation, the ions are clustered close to the surface rather than being isotropically distributed through the layer. Thermal annealing is needed to activate and distribute those ions to some useful depth that is controlled by the annealing temperature and time. The activation anneal described in this work was designed to diffuse the ions no further than 100 nm. However, while rapid thermal annealing seemed great for this process in theory, it actually caused a significant amount of damage to the pSi layer that became apparent after the final VHF etch, as illustrated in Figure 3.10.

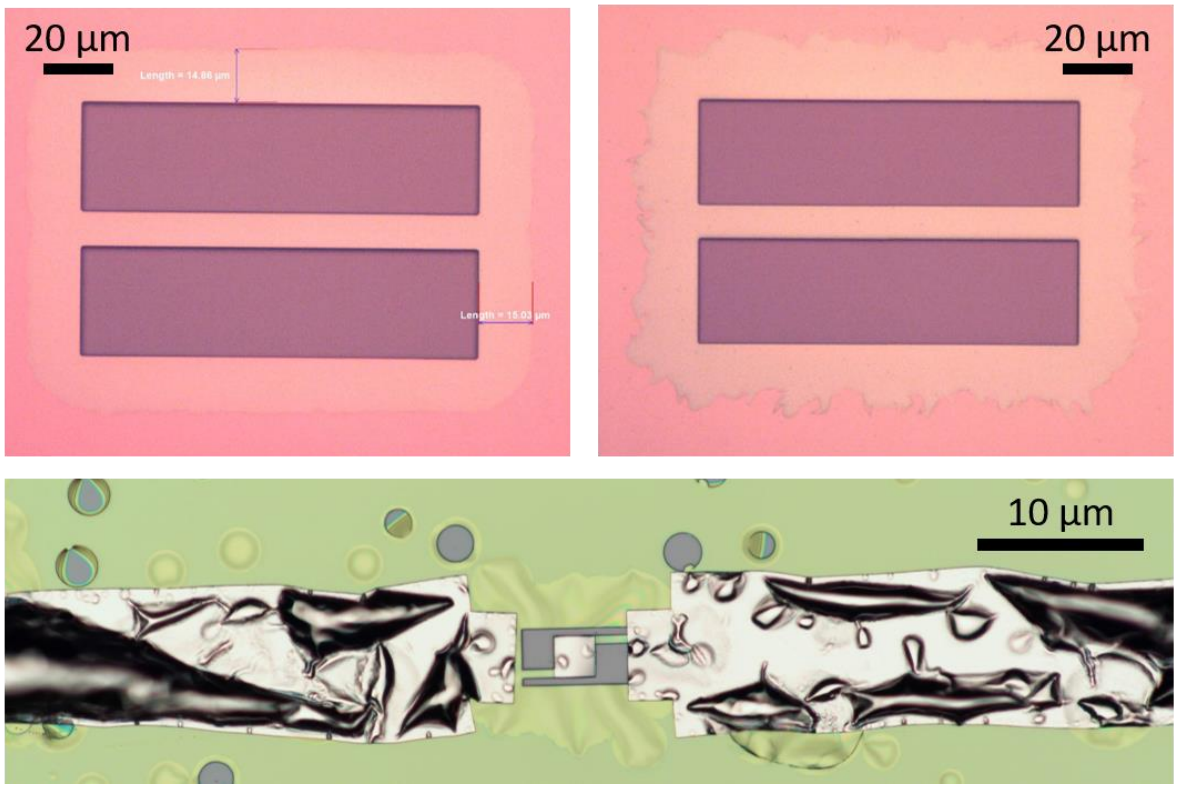


Figure 3.10 Optical micrographs of various pSi membranes post-vapour HF release from the underlying substrate. Both top images are nonporous test structures (the light pink line in between two gray rectangles) have been subjected to vapour HF etching. The light pink area is the pSi film, the gray rectangles are the exposed base wafer, and the light pink halo is the "undercut" region where the VHF etch removed SiO_2 from below the top film. The top right sample was rapid thermal annealed (RTA) prior to VHF, while the top left sample was not. The edge of the undercut region was noticeably rougher for the RTA-treated sample, indicating some damage was done by the anneal.

Figure 3.10, continued:
In the bottom image, a fully fabricated nonporous device is shown. This sample was subjected to both ion implantation and rapid thermal annealing (RTA) to activate the dopants. After the VHF etch, RTA-treated samples showed significant large holes and pinholes, warping of the Al pads, and uneven etching undercuts. There is a color difference (pink vs. yellow-green) because the top and bottom images came from two different lots of pSi on oxide wafers.

The RTA treated samples after VHF etching were visibly damaged. A possible reason for this damage is that 1000 °C is above the degradation temperature for SiO_2, based on the Ellingham diagram for Si/SiO_2[18]. It is possible that the underlying oxide, combined with trace amounts of O_2 in the RTA chamber atmosphere, partially oxidized the pSi layer along the grain boundaries. Any oxidized areas of the pSi film would have then dissolved in the VHF etch, leading to pinholes and etch damage across the film, which is what we observed. Another possibility is that there was an O_2 leak into the RTA tool, which would have the same end result of partial oxidation defects in the pSi and subsequent VHF damage.

The issue of RTA damage during dopant activation was resolved by doing a slower, lower temperature dry anneal in a thermal vacuum at 900 °C for 30 minutes total. No pinhole damage was observed on furnace-annealed samples after the VHF step in future work.

3.6.5. Membrane collapse

Many of the process issues described thus far degraded the mechanical integrity of our suspended devices, including etch-damage when removing the hard mask, oxidation damage during RTA, and large defects caused by imperfections in the BCP film. As a result, the membranes tended to sag and make contact with the base wafer after the BOX layer was removed, as shown in the bottom of Figure 3.11. The sagging membranes made thermal contact with the base substrate and consequently could not be measured. We devised a way to only support the membranes in order to make them measurable using support pillars. The VHF process etches the

SiO_2 from the exposed areas inwards. The porous legs and edges of the membranes were released quickly, while the SiO_2 below the Al pad etched more slowly. The etch was stopped after most of the membrane was fully released to leave a small SiO_2 support pillar below the central Al pad only. While the presence of this pillar degraded measurement quality by providing thermal contact to the base substrate, it made such measurements possible.

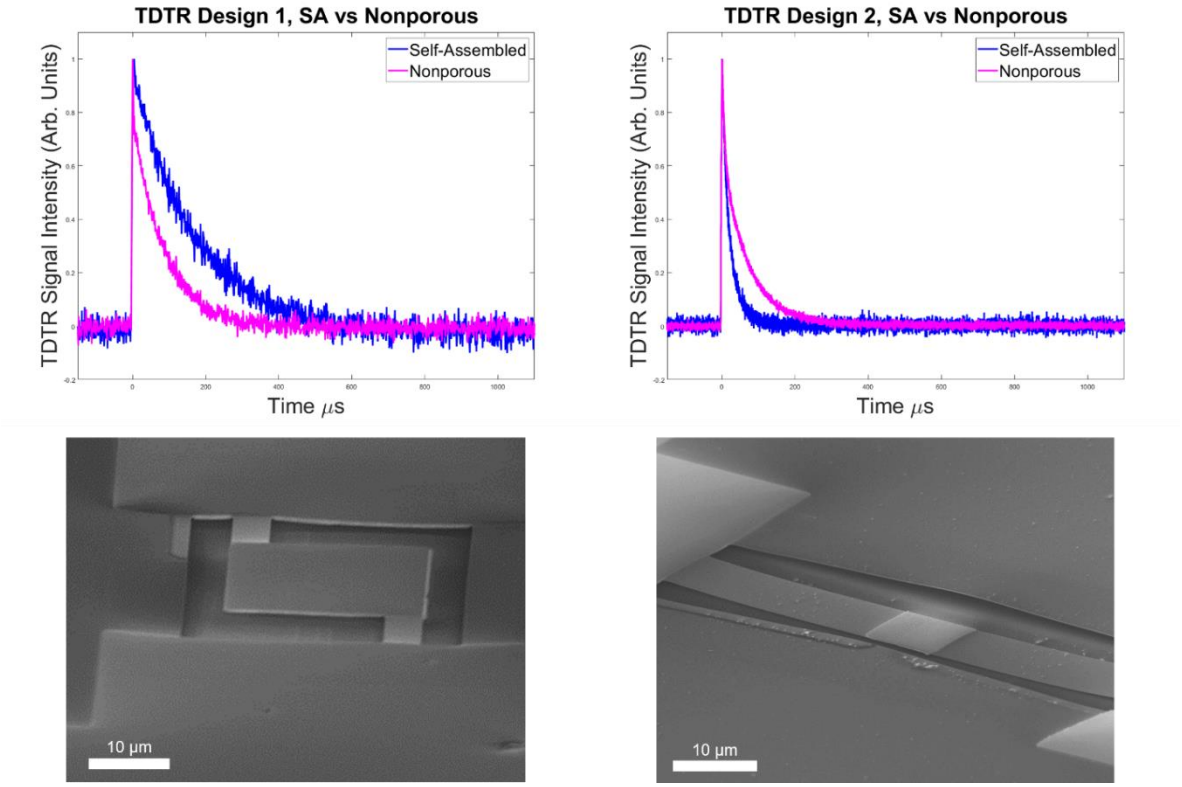


Figure 3.11 Top: TDTR measurements result for porous and nonporous suspended S1 compared to S2 devices.

The impact of membrane contact with the base substrate on the thermal measurements is shown in Figure 3.11. Thermal dissipation should occur more slowly through the nanostructured PnC than the control membranes, meaning that PnC should have a larger decay constant. However, the decay time of the S2 PnC devices was faster (21 ms) than the nonporous control membranes (71 ms). The thermal conductivity calculated from TDTR for the S2 control device was 9.5 W/mK

which is consistent with the literature for thin film pSi[19]. Using the same method to calculate thermal conductivity for the S2 PnC membrane, we obtained 54 W/mK, which is far too large to be accurate. This indicates that the porous PnC membrane sagged to touch the base substrate, which became the primary pathway for thermal dissipation rather than the device.

The mechanical stability of our Si-based membranes was significantly improved in future designs after process modifications that eliminated or resolved the processing challenges described throughout this chapter. These improvements are described in detail in Chapter 5 for monocrystalline Si suspended PnC membranes.

3.7 References

1. Maldovan, M. Sound and heat revolutions in phononics. *Nature* **503**, (2013).

2. Stoykovich, M. P. *et al.* Directed Self-Assembly of Block Copolymers for Nanolithography: Fabrication of Isolated Features and Essential Integrated Circuit Geometries. (2007). doi:10.1021/nn700164p

3. Thermal phonon engineering by tailored nanostructures - IOPscience. Available at: https://iopscience-iop-org.proxy.uchicago.edu/article/10.7567/JJAP.57.080101/meta. (Accessed: 17th September 2020)

4. Heino, P. Dispersion and thermal resistivity in silicon nanofilms by molecular dynamics. *Eur. Phys. J. B* **60**, 171–179 (2007).

5. Hori, T. & Shiomi, J. Tuning phonon transport spectrum for better thermoelectric materials. *Science and Technology of Advanced Materials* **20**, 10–25 (2019).

6. Wang, X. & Huang, B. Computational Study of In-Plane Phonon Transport in Si Thin Films. (2014). doi:10.1038/srep06399

7. Tambo, N. *et al.* Ultimate suppression of thermal transport in amorphous silicon nitride by phononic nanostructure. *Sci. Adv.* **6**, eabc0075 (2020).

8. Zhou, C. *et al.* Cite This: ACS Nano 2020, 14, 6980−6989 ACS Nano 2020, 14, 6980−6989 Downloaded via UNIV OF CHICAGO on. (2020). doi:10.1021/acsnano.0c01463

9. Yu, J.-K., Mitrovic, S., Tham, D., Varghese, J. & Heath, J. R. Reduction of thermal conductivity in phononic nanomesh structures. *Nat. Nanotechnol.* | **5**, (2010).

10. Tang, J. *et al.* Holey silicon as an efficient thermoelectric material. *Nano Lett.* **10**, 4279–4283 (2010).

11. Verdier, M., Anufriev, R., Ramiere, A., Termentzidis, K. & Lacroix, D. Thermal conductivity of phononic membranes with aligned and staggered lattices of holes at room and low temperatures. *Phys. Rev. B* **95**, 205438 (2017).

12. Ruiz, R. *et al.* Density multiplication and improved lithography by directed block copolymer assembly. *Science* **321**, 936–939 (2008).

13. Richards, P. L. Bolometers for infrared and millimeter waves. *J. Appl. Phys.* **76**, 1–24 (1994).

14. Williams, K. R., Gupta, K. & Wasilik, M. Etch rates for micromachining processing - Part II. *J. Microelectromechanical Syst.* **12**, 761–778 (2003).

15. Weisbord, I., Shomrat, N., Azoulay, R., Kaushansky, A. & Segal-Peretz, T. Understanding

and Controlling Polymer-Organometallic Precursor Interactions in Sequential Infiltration Synthesis. *Chem. Mater.* **32**, 4499–4508 (2020).

16. Zhou, C. *et al.* FULL PAPER www.afm-journal.de Fabrication of Nanoporous Alumina Ultrafiltration Membrane with Tunable Pore Size Using Block Copolymer Templates. (2017). doi:10.1002/adfm.201701756

17. Segal-Peretz, T. *et al.* Quantitative Three-Dimensional Characterization of Block Copolymer Directed Self-Assembly on Combined Chemical and Topographical Prepatterned Templates. *ACS Nano* **11**, 1307–1319 (2017).

18. *Ellingham Diagrams*.

19. Nomura, M. *et al.* Impeded thermal transport in Si multiscale hierarchical architectures with phononic crystal nanostructures. *Phys. Rev. B* **91**, 205422 (2015).

Chapter 4: Porosity characterization as a ultrasensitive tool for measuring chemical dry etch rate differences in doped Si

4.1 Introduction

Ion implantation is a robust and established method to customize the electrical properties of semiconductor materials in device fabrication. For technologies such as thermoelectric devices and bolometric IR sensors, it is critical to have low electronic noise, low heat capacity in the case of the bolometers, and low thermal conductivity (for bolometric sensors) for good performance[1].

It is useful to consider figures of merit (FOM), which are a measure of device performance, to better understand the purpose of ion implantation in thermoelectric and IR-sensing devices. For thermoelectrics, an important FOM is the ZT factor, which is written as $ZT = S^2\sigma/\kappa$, where S is the Seebeck coefficient, T is the temperature, κ is the thermal conductivity, and σ is the electrical conductivity[2]. For IR sensors, the responsivity R_v of a single IR pixel is a useful FOM and can be written as $R_v = I_b\alpha R\eta P_0/G(1+\omega^2\tau^2)^{0.5}$, where I_b is the bias current through the pixel, α is the temperature coefficient of resistance, P_0 is the amplitude of modulated IR radiation power falling on the pixel, τ is the thermal response time, ω is the angular frequency of modulation of the radiation, η is the absorbance of IR sensitive films, and G is the thermal conductance of the support structure[3]. Thus, for both thermoelectrics and IR sensors, the performance of the device is inversely proportional to the thermal properties of the device materials. Therefore, minimizing the thermal properties is a robust approach for optimizing the overall device performance.

As α, η, σ, and κ are typically material dependent properties and are difficult to optimize independently, designing and fabricating high efficiency, cost-efficient room-temperature thermoelectric and bolometric devices remains a challenge. Silicon is a material with a lot of potential to overcome some of these technological challenges due to its compatibility with a massive range of nanolithographic processes, availability, and ease of doping. The major

disadvantage of using Si to fabricate such devices is its large native thermal conductivity. However, recent development in phononic crystal fabrication has made it theoretically possible to engineer the thermal and electronic material properties of Si independently, as we discussed in Chapter 3.

The electrical properties of Si can be sensitively tuned by ion implantation[1,4,5]. Then, a nanostructure can be created from the doped Si that can significantly reduce the thermal conductivity of the Si by 80-90% or more of the bulk values[6–10]. The nanostructure dimensions are capable of interfering with phonon propagation but are too large to significantly affect the electrical properties. In this way, the electrical and thermal conductivities of Si can be engineered and customized independently. For bolometric sensors, low thermal conductivity supports are critical to minimize thermal noise from the bulk substrate and to increase the sensitivity. Doped monolithic Si devices are desirable for this application because, in addition to the aforementioned thermal and electronic customizability, it eliminates the issue of thermal boundary resistance between the sensor and the substrate[1].

However, combining ion implantation with a fabrication process for an ultrafine nanostructure is not without challenges. Ion implantation has well-established effects on the dry etch rates of silicon materials, which is increasingly consequential as the dimensions of modern semiconductor devices continue to shrink. In this section, the fabrication and design challenges that arise from incorporating doped Si into the fabrication process for a nanostructured IR sensor will be discussed. In this work, doped Si nanostructures were fabricated as a part of a broader study into using phononic crystals (PnCs) to enhance the sensitivity of an IR sensor. The PnCs were created by using block copolymer (BCP) cylinders as template for pattern transferring a nanostructure into Si. A rectangular membrane was then lithographically defined and released from the base substrate to be thermally isolated. During this fabrication process, we found that

our suspended devices would often break selectively on one side. Upon porosity analysis, we discovered that the etching rate was notably larger for the n-type regions than p-type or undoped regions. As a result, the n-doped legs of our membranes were had significantly larger porosity than the p-doped legs, which consistently led to mechanical failure.

While differences in vertical etch rate in p- and n-type Si have been previously documented, very few details have been reported about the lateral dry etch rate in doped Si. Similarly to what has been reported for vertical etching rates, we believe that the origin of etch rate variation between n- and p- doped Si is electrostatic in nature. The electronic structure of the doped Si, the bias of the plasma etchers, and the volatile etching byproducts at the surface are all believed to contribute to variations in etch rate. While studying the precise mechanisms behind these phenomena is beyond the scope of this work, we believe that porosity analysis of a nanostructure is a robust new method for assessing extremely small differences in the chemical etch rate of materials that are conventionally assumed to etch at similar vertical rates. We believe our proposed etch rate analysis method could be critical for designing fabrication processes for doped Si nanostructures, as slight variations that were within process tolerance at the micron scale become significant at the nanometer scale.

4.2 Experiment

4.2.1 Materials

Silicon-on-insulator (SOI) 200 mm wafers were purchased from Silicon Valley Microelectronics (USA) with the following specifications: <100> monocrystalline Si, 100 nm; buried oxide (BOX), 3 μm; handle wafer, 725 μm; wafer diameter, 200 mm. Wafers were used without further cleaning. Acetone (≥ 99.5%), isopropyl alcohol (≥ 99.9%), n-methyl pryrrolidinone (NMP, ≥ 99.0%), toluene (≥ 99.5%), and n-amyl acetate (≥ 99.0%) were purchased

from Sigma Aldrich and used as received. For general photolithography, AZ MiR703 (PR703) positive photoresist and AZ MIF300 (MIF300) developer were purchased from AZ Materials. For fabricating Al thermal contacts, n-LOF2020 (PR2020) negative photoresist was purchased from AZ Materials. For EBL, AR-P 6200.04 (ARP) resist was purchased from Allresist. Trimethylaluminum (TMA) and all lithography resists and solvents were provided by the Pritzker Nanofabrication Facility.

The BCP used in the study was a cylinder-forming polystyrene-block-poly(methyl methacrylate) (M_n 20k-b-50k, denoted as C2050, bulk period p = 37.5 nm) that was purchased from Polymer Source and used as received. For perpendicular BCP assembly, wafer were first coated with a random poly(styrene-r-(methyl methacrylate)) copolymer (P(S-r-MMA)) mat that was designed to be energetically neutral to both blocks of the PS-b-PMMA. Solutions of all polymers used in this work were filtered prior to spin-coating using a 1 mL polypropylene syringe and an mdi Membrane Technologies PTFE syringe filter with 0.2 μm pore size. All polymer solutions were prepared in toluene.

4.2.2 Sample Preparation

To fabricate suspended membranes with selective p- and n-doping, SOI wafers were used instead of pSi-on-insulator wafers due to substrate availability and changes in the direction of the work. The device fabrication for the doped SOI devices was otherwise identical to the method described for doped pSi membranes in Chapter 3.

In addition to functional, full-fabrication membranes, a variety of test chips were prepared to test only the hole-etching step for p- and n- implanted Si, along with undoped Si, amorphous Si, and polySi. The pSi and aSi substrates were fabricated for posterity and were not part of the main focus of this work. To prepare the doped chips, each 200 mm SOI wafer was first cut into 45 mm^2

chips and sent for ion implantation according to the same parameters described in Chapter 3. For doped SOI, each chip was either p- or n- implanted. Additional 45 mm^2 chips of undoped SOI were also prepared. For the undoped aSi and pSi, the 100 mm wafers were diced into 22.5 mm^2 chips. After ion implantation, the p- and n- implanted 45 mm^2 chips were activated by annealing in a dry furnace at 900 °C for 30 minutes. After activation, all the 45 mm^2 SOI chips were cut into 22.5 mm^2 chips. Etching tests were conducted on 22.5 mm^2 chips for the n-doped SOI, p-doped SOI, undoped SOI, undoped pSi, and undoped aSi substrates.

Next, all samples were prepared with the C2050 thin film as described in Chapters 3 and 5. After BCP annealing and SIS, the 22.5 mm^2 samples were mounted via thermal tape on a Si carrier wafer and lightly O_2 plasma etched for 10 minutes in a PlasmaTherm RIE to remove the PS cylinders. Immediately after this etch and without breaking vacuum in the tool, a Cl_2 chemistry plasma etch was used to transfer holes from the SIS structure into the underlying Si.

After etch transfer, the SIS structure was stripped an 80C piranha (conc. H_2SO_4: 30% H_2O_2 7:3) etch for 45 minutes, then rinsed copiously with DI H_2O and dried with a N_2 gun. Next, samples were subjected to VHF etching to selectively remove the BOX layer. Finally, VHF-etched samples were inspected in top-down SEM for porosity calculation.

4.3 Results and discussion

To test the reproducibility of the difference in porosity in etched p- and in-implanted polySi, we tested etching in single-crystal doped Si. Due to substrate availability, monocrystalline SOI wafers were used for these follow-up experiments, as both polySi and Si are susceptible to the same etching chemistries. SEM micrographs of the full-fabrication Si membranes are shown in Figure 4.1.

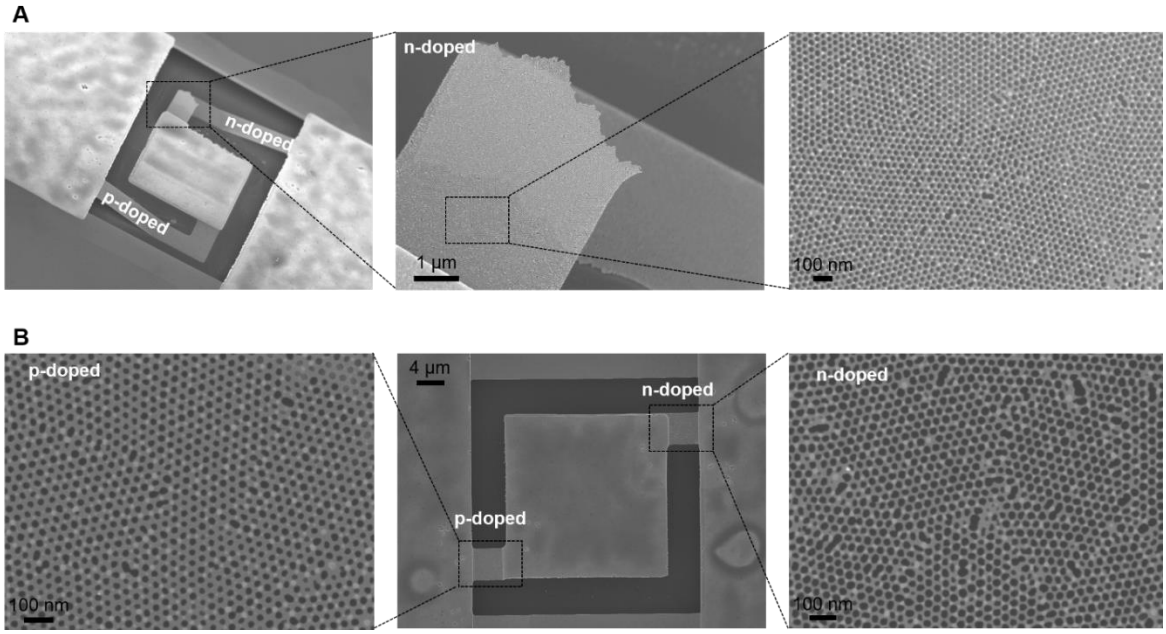


Figure 4.1 SEM micrographs of suspended nanoporous membranes fabricated from single crystal silicon. Two different device designs are shown in A and B. In A, a membrane with long, L-shaped legs is shown, while in B a membrane with short, linear legs is shown. Each image to the right in A is a zoom of the previous image. Magnified views of the n-implanted leg of the membrane are shown only. The membranes in A broke selectively on the n-doped side, resulting in membrane collapse. This was likely due to the significantly larger porosity in the n-doped Si vs the p-doped Si after the same amount of etch time for both, weakening the mechanical stability of the n-implanted side. Membranes like in B with shorter, linear legs, had a higher survival rate despite the differences in porosity and mechanical strength.

Porosity was calculated using SEM images of samples post-VHF etching. When the BOX layer is present in SEM imaging, charge builds around the edges of the holes, resulting in a bright ring that makes the porosity appear smaller. Removing the BOX layer prior to SEM characterization eliminates this effect. Additional details about BOX layer effects on perceived porosity in SEM are described in Chapter 5. The method for porosity calculation is also described in Chapter 5. From porosity analysis for the p- and n- doped legs of the membranes shown in Figure 1, we determined that, for the same etching time, the porosity for p- and n-doped SOI legs were 34.0% and 46.5%, respectively. These porosities correspond to hole radii of approximately 11.3 nm and 13.3 nm for the p- and n-doped legs, respectively. While an average difference of 2

nm is small, the effect on the final porosity is significant, resulting in a difference of 12.5%. At this length scale, such a large porosity differential not only affects interpretation of IR sensitivity or thermal conductivity measurements, but also the mechanical stability of the membrane as shown in Fig. 4.1.

To investigate the effects of doping on the etch rate of holes into Si more methodically, nanoporous p-doped, n-doped, and undoped SOI test substrates were prepared. All substrates were fabricated from the same SOI wafer with a 100 nm thick Si top layer stacked on top of a 3 μm thick BOX layer, as described in Section 4.2.1. For the p- and n- doped substrates, only the top monocrystalline Si layer was doped.

First, the p- and n- doped SOI substrates were ion implanted and thermally annealed to activate the dopants as described in Section 4.2.2. Then, each of the 5 substrate types was diced into 22.5 mm^2 chips. Next, each chip was prepared with the neutral 67S mat, then the C2050 BCP thin film, and annealed to form BCP cylinders. For processing simplicity, the BCP was self-assembled rather than direct-self assembled. Then, the samples were subjected to SIS to infiltrate the PMMA block selectively with AlO_x, turning the film into a hard mask for etching. After SIS, the samples were lightly etched in O_2 plasma to selectively remove the PS cylinders, resulting in a nanoporous AlO_x hard mask. Then, a 1 min Cl_2 chemistry plasma was used to etch the holes completely through the 100 nm of each Si-type substrate. All substrates were etched simultaneously in order to be able to compare results between substrate types. After hole etching, a piranha etch was used to remove the SIS structure, and the samples were then cleaned in DI H_2O and dried with a N_2 gun. Finally, all samples were subjected to a 1800s VHF etch to selectively remove the underlying BOX layer. Post-VHF, samples were inspected in top-down SEM using a Carl Zeiss Merlin FE-SEM and porosity was calculated.

Images of the nanoporous SOI substrates are shown in Figure 4.2. From these images, it is clear to see that the apparent porosity of the nSOI sample is noticeably larger than all the other substrates. From porosity analysis, the order of porosity from largest to smallest was nSOI (3.1%), SOI (27.7%), then pSOI (25.5%).

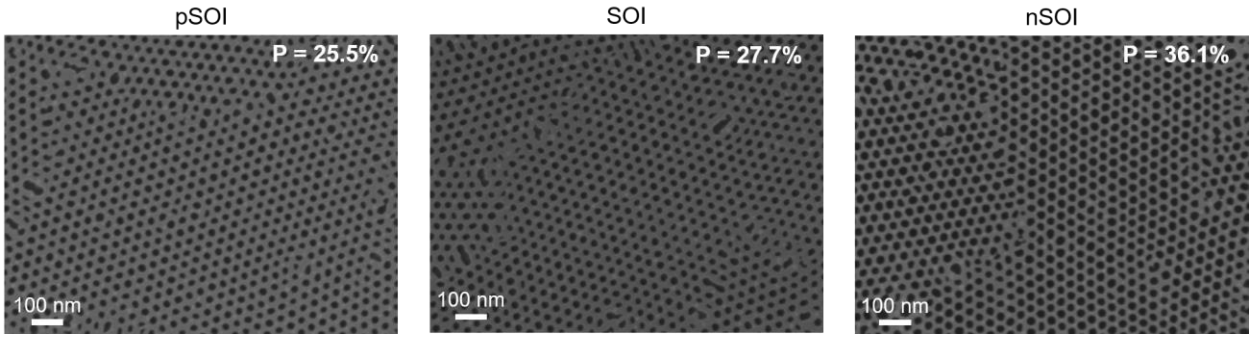


Figure 4.2 SEM micrographs of the nanoporous p-doped, n-doped, and undoped SOI substrates. From left to right, a clear trend of increasing porosity is observable, with n-doped Si having the largest porosity and p-doped Si having the smallest porosity. As all substrates were etched simultaneously for the same amount of time, the porosity difference is a result of differences in the chemical etching rate of doped Si in plasma etching.

It is well established in the literature that the etch rates of p- and n-type Si in F- and Cl-chemistry plasma differ significantly for heavily doped (~$10^{19\text{-}20}$ ions/cm^3) Si[11]. Generally, heavily n-doped Si and pSi have been documented to etch as many as 15-25 times faster than undoped Si, and more rapidly than lightly doped n-type Si[12]. Lightly doped (~10^{15} ions/cm^3) p- and n- type Si have been shown to have similar etch rates, while heavily doped p-type Si and pSi etches more slowly than heavily n-doped, undoped, and lightly doped p- and n- type Si and pSi[1,2].

Mechanistically, Haarer et al reported that dopant type affects the etch rate of Si due surface charge during the etch[11]. For F chemistry plasmas, it is thought that exposure of Si to XeF_2 results in the formation of a fluorosilyl group on the surface, which causes the affinity level for F at the surface to lie below the valence band. This fluorosilyl layer contains negative ions. The number of negative ions N- on the surface is dependent on the thickness of this insulating fluorosilyl layer,

decreasing as the layer thickness increases. N- is also affected by Si doping, and is larger for n-doped Si. The electronic field E around the sample is proportional to N-, and when N- is large, E is large and vice versa. When N- is large, the valence band edge move towards the Fermi level, bending the bands significantly.

For heavily p-doped Si, the Fermi level is inside the valence band, and there is little band bending upon dry etching. Similarly, for lightly p- or n- doped Si, and for undoped Si, little band bending occurs upon etching, and the Fermi level is near the valence band. For heavily n-doped Si, large N- results in significant band bending, resulting in the Fermi level being near the conduction band. Due to the creation of this large potential difference, heavily n-doped Si etches more quickly than undoped and p-doped Si. While this study focused their discussion on F-chemistry plasmas, the authors suggested that similar etching trends would apply for non-crystallographic Cl plasma etching provided that negative ions at the surface were the driving force for etch rate[11].

The porosity trends visible in our etching test results are directly in line with the phenomena reported in the literature, and can also be interpreted as an etch rate based on the average hole radii for each sample. Given the total etch time of 1 min, the nSOI etched at 0.199 nm/s, the pSOI at 0.167 nm/s, and the SOI at 0.175 nm/s. The order of sample types from largest to smallest etch rate was nSOI, SOI, then pSOI. This is the same trend observed for sample porosity. Our results agree with the established literature in that the n-type Si etched significantly faster than the undoped Si, and the p-type Si etched more slowly than both n-type and undoped Si.

It is important to note that there are two general regimes of etching in plasma dry etching: chemical etching and ion assisted etching. In chemical etching, a chemical reaction occurs between the substrate and the reactive plasma, forming a volatile compound that escapes the

surface, thereby etching it. This form of etching is isotropic. In ion-assisted etching, ions physically bombard the surface, ablating it and thereby etching it. This type of etching is anisotropic. By measuring the porosity of samples and analyzing the hole radii from a top-down perspective, we are only measuring lateral etching that occurred, which is primarily chemical in origin. We believe that the differences in etch rate we measured represent small differences in the lateral chemical etch rate of the different Si substrate types.

While the differences in the lateral etch rate in Si as a function of doping vary slightly, the overall impact of these small differences becomes significant when considering the impact of slight differences on the porosity. While the small differences in etch rate affect the radius of the holes, the porosity is a function of radius squared, meaning that small changes in radius have an amplified effect on the porosity. This is significant when fabricating ultrafine nanoporous structures such as those presented in this work, where the pitch of the holes is comparable to the hole diameter, and the neck widths approach 10 nm. As demonstrated in Figure 3.1, for nanostructures with regions of p- and n- doping, these small differences in etch rate can present a massive design challenge. Because n-doped Si etches much faster than p-doped Si, the n- and p-doped regions of the device must be etched separately to ensure that both regions have the same pore dimensions (and by extension, porosity). This important from both a mechanical stability and a device performance perspective. For the phononic crystals shown in Figure 1, the porosity of the sample is an important variable incorporated into the calculations to determine the thermal conductivity of the nanoporous membranes. If the porosity in the n-doped and p-doped parts of the device differ significantly, analysis and interpretation of the results is prohibitively complicated. It is therefore important to be aware of the differences in the relative etch rates of doped Si when designing ultrafine nanostructures for various semiconductor devices with dimensions on the order of a few

tens of nm. While these trends in vertical etch rate for doped Si have been extensively reported, we believe that this is the study of the lateral (and predominantly chemical) etch rate dependence on dopant type. We also believe that this is the first report to present porosity measurements of a hexagonal nanostructure to quantify these slight differences in etch rate that would be unmeasurable in any other way.

This technique has potential to directly measure small variations in chemical etch rate for a wide range of materials beyond doped Si. In addition to measuring the etch rate differences between n- and p- doped Si and undoped Si, we conducted several other tests on different types of Si: amorphous (aSi) and polycrystalline (pSi) silicon. Information about the aSi and pSi substrates is available in Section 4.2.1. Images of the aSi and pSi nanostructures compared to the undoped SOI nanostructure are shown in Figure 4.3.

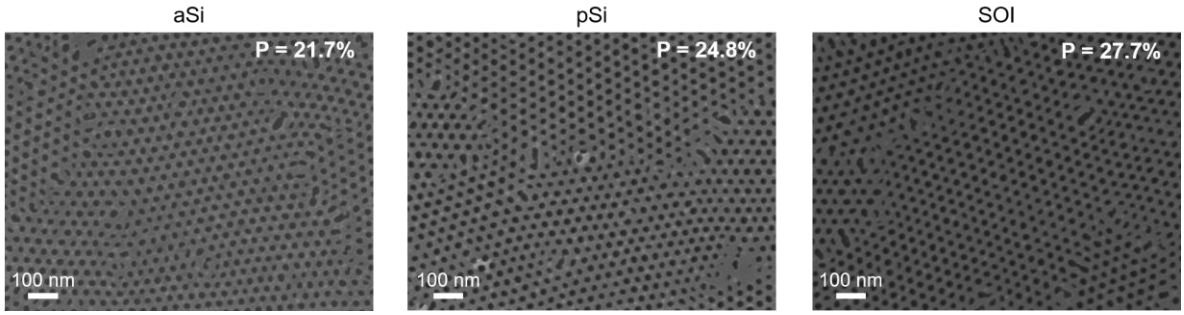


Figure 4.3 SEM images of nanoporous amorphous, polycrystalline, and single-crystal Si nanostructures. Porosity analysis showed that the aSi had the smallest porosity, while the undoped SOI had the largest porosity.

For undoped aSi, pSi, and SOI, non-crystallographic dry etch rates are relatively similar[13]. Given the total etch time of 1 min, the aSi etched at 0.157 nm/s, the pSi etched at 0.165 nm/s, and the SOI etched at 0.175 nm/s. The order of sample types from largest to smallest etch rate was pSOI, pSi, and aSi, which matches the trend in porosity from largest to smallest as well. Interestingly, a clear trend emerged in the etch rates for aSi, pSi, and SOI that was similar in

magnitude to etch rate variations across the doped and undoped Si. The technique presented separates the chemical etching behaviour from the ion etching behaviour by only examining small variations in the lateral etch rate. This becomes meaningful as semiconductor device sizes shrink to tens, and even single, nanometers in size. While thoroughly investigating these etching rate variations between amorphous, polycrystalline, and monocrystalline Si was beyond the scope of this work, we believe that using nanoscale porosity as a sensitive means of measuring such slight differences in chemical etch rate enables experiments like this and is a valuable approach for understanding material properties during dry etching at the ultrafine nanoscale. In this case, we believe our metrology technique could be used to study the impact of crystal structure on nanoscale variations in dry etch rate, which could not be easily evaluated in any other way.

4.4 Conclusions

In summary, we documented the lateral (and predominantly chemical) dry etch rates for a variety of doped and undoped Si substrates. We developed a method for using top-down porosity measurements of a hexagonal nanopore array to measure the small differences in etch rate between different substrates. Our results are in agreement with previous reports on vertical dry etch rate differences in p-doped, n-doped, and undoped Si. Our findings also agree with the literature understanding that chemical etch rate is sensitive to substrate type.

These observations provided valuable information that helped us improve our process design. Primarily, we learned that it is necessary to etch the p- and n-implanted membrane components separately in order to fabricate devices with uniform porosity post-ion implantation, with a shorter etching time for the n-implanted side. Next, we learned that nanoscale hole etching is a robust method for analyzing the nanoscopic differences in chemical etch rate in different kinds of Si. The change in porosity is a function of the radius of the hole squared, meaning that small

differences in etching rate are amplified when analyzing the porosity of a sample and are therefore more easily inferred from top down image analysis. We believe this method is potentially suitable for measuring small differences in dry etch rate between any combinations of other substrates, and could potentially provide a means of studying and quantifying etch rate differences that were previously unmeasurable in any way.

4.5 References

1. Richards, P. L. Bolometers for infrared and millimeter waves. *J. Appl. Phys.* **76**, 1–24 (1994).

2. Maldovan, M. Sound and heat revolutions in phononics. *Nature* **503**, (2013).

3. Saxena, R. S. Figure 1. Schematic block diagram of a thermal detector (microbolometer). *Def. Sci. J.* **59**, 580–589 (2009).

4. G. Dearnaley. Ion Implantation. *Nature* 701–705 (1975). doi:10.1016/B978-0-323-60984-5.00062-7

5. Tokuyama, T. Trends in ion implantation in silicon VLSI technology. *Nucl. Inst. Methods Phys. Res. B* **19**–**20**, 299–306 (1987).

6. Tambo, N. *et al.* Ultimate suppression of thermal transport in amorphous silicon nitride by phononic nanostructure. *Sci. Adv.* **6**, eabc0075 (2020).

7. Zhou, C. *et al.* Cite This: ACS Nano 2020, 14, 6980−6989 ACS Nano 2020, 14, 6980−6989 Downloaded via UNIV OF CHICAGO on. (2020). doi:10.1021/acsnano.0c01463

8. Yu, J.-K., Mitrovic, S., Tham, D., Varghese, J. & Heath, J. R. Reduction of thermal conductivity in phononic nanomesh structures. *Nat. Nanotechnol.* | **5**, (2010).

9. Lee, J., Lim, J. & Yang, P. Ballistic Phonon Transport in Holey Silicon. *Nano Lett* **15**, 48 (2015).

10. Tang, J. *et al.* Holey silicon as an efficient thermoelectric material. *Nano Lett.* **10**, 4279–4283 (2010).

11. Winters, H. F. & Haarer', D. *In8uence of doping on the etching of Si(111). PHYSICAL REVIEW B* **36**,

12. Ogryzlo, E. A., Flamm, D. L., Ibbotson, D. E. & Mucha, J. A. The etching of doped polycrystalline silicon by molecular chlorine. *J. Appl. Phys.* **64**, 6510 (1988).

13. Hailer, I., Lee, Y. H., Nocera, J. J. & Jaso, M. A. *Selective Wet and Dry Etching of Hydrogenated Amorphous Silicon and Related Materials*.

Chapter 5 The use of directed self-assembly to generate precise, ultra-fine phononic crystals for determining the effect of superstructure orientation on thermal conductivity

Abstract

Directed self-assembly (DSA) of block copolymer films was used to generate silicon phononic crystals with sufficient precision to probe the effect of phononic crystal orientation on thermal conductivity. The silicon phononic crystals were made using DSA as a template to pattern transfer hexagonally close-packed holes into Si. The pitch of the holes was 37.5 nm, and the neck between holes was 12.1-12.3 nm. The orientation of the hexagonal array of holes with respect to the direction of heat transport was changed from 0° to 30° by changing the orientation of the chemical pattern used for DSA. The change in array orientation caused different pathways to be seen by the thermal phonons. The thermal conductivity of the membranes was measured by time-domain thermoreflectance. The geometry of the Si nanoporous membrane was found to have a measurable effect on the thermal conductivity, which was likely due to phonon directionality being affected by the nanostructures. The mechanism for κ reduction was probed by molecular dynamics simulations and was found to stem primarily incoherent scattering.

5.1. Introduction

The rapid reduction in semiconductor pattern size over the past several decades has led to technological advances that have revolutionized the design and capabilities of electronic devices[1,2]. As feature sizes have shrunk, devices have become more susceptible to thermal degradation because the thermal properties are affected by both the length scales of the devices and their intrinsic material properties[1,3,4]. As a result, thermal management has emerged as an important design consideration, especially for applications such as thermoelectric devices and infrared (IR) sensors, which require thermal isolation and low thermal conductivity (κ)[1,5,36].

It is also important to consider thermal properties for semiconductor applications in which very specific sizes and shapes of various materials are layered together from electronic components such as transistors. Such devices are typically composed of structures that have dimensions comparable to or smaller than the average mean free path (MFP) of thermal phonons. Because of the relative length scales of device structures and phonon MFPs, classical models of heat transport and diffusion are not expected to adequately capture the behavior of heat transport in nanoscale materials[3].

A number of studies in recent years have investigated the behavior of thermal phonons in semiconductor nanostructures, which are typically referred to as phononic crystals (PnCs); the latter are defined as any periodic array of elastically mismatched materials, e.g. a periodic array of voids in crystalline Si. Results reported in the literature for κ in Si PnC nanostructures can be categorized by nanostructure geometry (usually square-[7–11] staggered square-[9,10], or hexagonal[11–15] close packed (HCP) holes), length scale of the nanostructure (~100 nm to >10 μm), and also by the measurement technique (e.g., time-domain thermoreflectance (TDTR)[12,13], 3ω[16], micro-electro-mechanical systems (MEMS))[8,17], measurement temperature (4–300 K), and finally by the fabrication method (e.g., e-beam lithography (EBL)[3,9–11], block copolymer (BCP) lithography[12–14], microsphere lithography[14], and nanowire lithography[8]). While many studies have investigated nanostructures with lattice pitch (*p*) and neck width (*n*) values ranging from ~100 nm to >10 μm, until recently the significant challenges posed by lithographic patterning features smaller than 50–100 nm have limited the availability of data at ultrafine length scales[7–9,11–15,18–23]. Microsphere lithography, EBL, and BCP lithography have all been used to fabricate nanostructures consisting of sub-100 nm diameter HCP holes. Lattices have been formed with p = 120 nm and n = 40–150

nm by EBL[11], with p = 140 nm by microsphere lithography[14], and with p = 34, 55, and 60 nm and n ~ 10-20 nm by BCP lithography[12,14,15].

In the literature two quantities have been used to discuss thermal transport in PnCs: the measured thermal conductivity of the material (κ_{mat}) and κ_{eff}, obtained from an effective medium model to account for the reduced volume due to the presence of voids. The κ_{eff} values from the studies carried out at 300K were in the range of 2–7 W/mK. EBL was also used to create a Si nanomesh structure with p = 34 nm and n = 18 nm that had κ_{eff} of ~2 W/mK[8]. These studies also reported surface area to volume (s/v) ratios ranging from of 0.03–0.06 nm^{-1} for an HCP lattice with $p = 120$ nm[11] to 0.14 for a Si nanomesh[8]. Based on these results, it appears that n, p, porosity (P), and s/v are the most critical design parameters when fabricating a low κ_{eff} nanostructured material. Although P is important, a strong reduction in κ_{eff} trends more strongly with n and s/v than any other parameters[11].

A number of studies have experimentally and computationally investigated how the orientation of the nanostructured pores with respect to the direction of heat flow affects κ_{eff} in PnCs[3,7,9–11,13,21,22,24]. There is a growing body of evidence indicating that the MFP of phonons in nanostructured Si can be measurably influenced by the geometrical arrangements of pores. Two general types of lattices have been commonly investigated: aligned lattices, where a contiguous pathway through the nanostructure is parallel to the direction of heat flow, and staggered lattices, where staggered holes are present in the path of heat flow, and there is no contiguous open pathway through the nanostructure. However, the majority of these studies have been experimentally limited to nanostructures with p and n larger than 100 nm and 40 nm, respectively, due to significant challenges in fabricating finer defect-free nanostructures. Reports of finer

nanostructures were unable to fabricate defect-free, isoporous structures with tunable configurations[8,12,14].

In this work, we present an approach to fabricate Si PnC nanostructures with HCP holes templated by BCP self-assembly (SA) and directed self-assembly (DSA) that allowed us to investigate dimensions below 40 nm. This work builds upon our previous work on amorphous silicon nitride [ref] where we showed that nanostructures cannot induce phonon directionality in amorphous materials[13,22]. The fabricated Si devices have p = 37.5 nm, n = 12.1–12.3 nm, P = 40-42%, and $0.02 < s/v < 0.133$. By rotating the orientation of the HCP lattice relative to the direction of heat flow through the devices by 30°, the pathway "seen" by phonons traveling through the nanostructure changed. In this way, we were able to examine whether, at these nanoscopic length scales, the configuration of the nanostructure had a measurable effect on κ_{eff} at room temperature. In addition, we carried out atomistic MD simulations for samples directly comparable with experiments that allowed us to interpret, at the microscopic scale, our experimental results. Our work extends the existing understanding of configurational effects of nanostructures on phonon transport into the 10–15 nm regime, and contributes to discussion of the following: (1) the magnitude of κ_{eff} reduction at 300 K, (2) the relative importance of n and s/v for designing low κ_{eff} ultrafine nanostructures, and (3) the effects of nanostructure configuration on phonon transport and directionality.

5.2. Experiment

5.2.1. Materials

Silicon-on-insulator (SOI) 200 mm wafers were purchased from Silicon Valley Microelectronics (USA) with the following specifications: <100> monocrystalline Si, 100 nm; buried oxide (BOX), 3 μm; handle wafer, 725 μm; wafer diameter, 200 mm. Wafers were used

without further cleaning. Acetone (≥ 99.5%), isopropyl alcohol (≥ 99.9%), n-methyl pryrrolidinone (NMP, ≥ 99.0%), toluene (≥ 99.5%), and n-amyl acetate (≥ 99.0%) were purchased from Sigma Aldrich and used as received. For general photolithography, AZ MiR703 (PR703) positive photoresist and AZ MIF300 (MIF300) developer were purchased from AZ Materials. For fabricating Al thermal contacts, n-LOF2020 (PR2020) negative photoresist was purchased from AZ Materials. For EBL, AR-P 6200.04 (ARP) resist was purchased from Allresist. Trimethylaluminum (TMA) and all lithography resists and solvents were provided by the Pritzker Nanofabrication Facility.

The BCP used in the study was a cylinder-forming poly(styrene)-*block*-poly(methyl methacrylate) (M_n 20k-*b*-50k, denoted as C2050, bulk period p = 37.5 nm) that was purchased from Polymer Source and used as received. Hydroxy-terminated polystyrene brush with a M_w ~6k (PS-OH) was purchased from Polymer Source and used as received. For perpendicular BCP assembly, samples were first coated with a random poly(styrene-*r*-(methyl methacrylate)) copolymer (P(S-*r*-MMA)) mat that was designed to be energetically neutral to both blocks of the PS-*b*-PMMA. P(S-*r*-MMA) was synthesized in-house, using glycidyl methacrylate as a cross-linker, azobisisobutyronitrile (AIBN) as an initiator, and styrene (S) fractions of 50–70%. It was experimentally determined that a 67% S mat, denoted 67S, promoted the highest pattern quality (and lowest pattern defectivity) for in- and out-of-plane assembly of C2050 with DSA. Details of the synthesis and analysis of P(S-*r*-MMA) are provided in Section 5.6.1. Solutions of all polymers used in this work were filtered prior to spin-coating using a 1 mL polypropylene syringe and an mdi Membrane Technologies PTFE syringe filter with 0.2 μm pore size. All polymer solutions were prepared in toluene.

5.2.2. Sample preparation

Each SOI wafer was diced using a DISCO Dicing Automatic Dicer into 12 45 × 45 mm^2 chips. The cutting direction was aligned to the <100> direction of the top layer of the Si. Each chip was designed to contain 14 1 cm^2 arrays, with each array comprising 49 membranes of one specific membrane design, resulting in a total of 49 x 14 = 686 individual membranes fabricated simultaneously on each chip. The fabrication process was carried out on the 45 x 45 mm^2 chips. Each 45 × 45 mm^2 chip was diced into 14 1 cm^2 samples prior to measurements of κ.

First, four sets of Au alignment marks were deposited for both photolithography and EBL. Cross markers (100 μm long × 40 μm wide) were used for photolithography, and positive 20 x 20 μm^2 squares were used for EBL. A Heidelberg MLA direct-write lithography system was used to pattern the alignment marks, an Angstrom EvoVac Electron-Beam Evaporator was used to evaporate Au, and a simple liftoff procedure in NMP was used to complete the alignment mark formation. Each alignment mark was 100 nm thick, and 10 nm Ti was used as an adhesion layer for the Au.

Next, the substrate was coated with the 67S mat, which was designed to be energetically neutral to both blocks of C2050 at the annealing temperature. To prepare the mat, a 0.3 wt% solution of 67S in toluene was spin-coated to a thickness of ~9.5 nm. The mat was cross-linked by annealing on a hot plate in a N_2 glove box for 15 min at 225 °C. Then, excess (unreacted) mat was rinsed from the sample by sonicating in toluene for 5 min. After annealing and rinsing, the neutral mat thickness decreased slightly to 8 nm.

The chemical patterns for DSA started with the 67S mat on the SOI chip, which was coated with 90 nm of ARP. An e-beam pattern of HCP 4 nm^2 dots with a period (L_S) of 75 nm was written using a Raith EBPG5000 Plus writer at a dose of 45,000 $\mu C/cm^2$ and a current of 2 nA. The

accelerating voltage of the beam was 100 kV and the beam current was 1 nA. Each patterned field of spots was 100 × 125 μm^2 in size. To prepare samples with different pattern rotation with respect to the long axis of the bridge, a rotation matrix was used to rotate and translate the coordinates using a 2-point basis. The e-beam patterns were then developed in n-amyl acetate for 1 min with agitation, then quenched and rinsed with IPA. After developing, the e-beam pattern was used as a mask to etch holes into the underlying 67S mat by a 15 s, low-power O_2 plasma etch using a PlasmaTherm reactive ion etcher (RIE). The e-beam resist was then stripped with NMP and toluene. Next, a 0.7 wt% solution of PS-OH in toluene was spin-coated onto the sample. The PS-OH was grafted onto the substrate by annealing at 225 °C for 30 min in a N_2 glove box. The PS-OH selectively grafted to the bare substrate but did not significantly graft to the 67S mat. After grafting, excess brush was removed by sonicating and rinsing the sample in NMP and toluene.

We built on previous reports of SA and DSA with C2050 to generate our SA and DSA structures [13,22,25]. A 2 wt% solution of C2050 in toluene was spin-coated directly onto the 67S mat or the chemical pattern for SA or DSA, respectively, to a thickness of 85 nm. Next, the samples were annealed at 270 °C for 2.5 h on a hot plate in a N_2 glove box. After 2.5 h, the samples were thermally quenched by placing them on a cool metal block.

Sequential infiltration synthesis (SIS) was performed with a Cambridge NanoTech Savannah thermal atomic layer deposition (ALD) tool to selectively infiltrate the PMMA block with vapor-phase precursors (TMA and DI H_2O) and nucleate a significant amount of AlO_x within the PMMA domain[26,27]. This resulted in a hybrid organic/inorganic PMMA/AlO_x film containing HCP PS cylinders, which we refer to as the SIS-PS structure.

After SIS, lithography was used to define specific regions for subsequent hole transfer into the underlying silicon. First, an Angstrom EvoVac E-Beam Evaporator was used to deposit 20 nm

protective layer of Au at a rate of 1 Å/s directly on top of the SIS-PS structure. Next, PR703 was spin-coated to a thickness of ~1 μm directly on top of the Au layer, then soft-baked for 1 min. A Heidelberg MLA Lithographer was then used to define 100 × 150 μm^2 areas where hole etching would occur, which were then developed for 1 min. The developed lithographic pattern was then baked for at least 3 h in a 120 °C oven to increase the adhesion of the photoresist to the Au. The Au was then removed from the pattern area by immersing the samples in Au etch for 30 s and then rinsing with deionized water, which exposed the underlying SIS-PS structure only in the patterned area.

Next, RIE was used to lightly etch the samples with an O_2 plasma and remove the PS cylinders from the exposed sample area, resulting in a nanoporous AlO_x SIS structure. This SIS structure was immediately used as an etch mask for a Cl_2/O_2 plasma that etched holes through the underlying Si. A 3 min O_2 plasma etch in a downstream asher was used to remove any etching residue from the photoresist. Then the PR703 was stripped by soaking in NMP at 80 °C for at least 1 h, followed by ultrasonication in NMP and IPA. The samples were then immersed in Au etch for 30s and rinsed thoroughly with DI H_2O to remove the protective Au layer. A hot piranha etch was used to remove the SIS structure and any remaining polymer, and then the samples were rinsed thoroughly with DI H_2O. Finally, the samples were cleaned in an O_2 plasma in a downstream asher for 3 min at 70 °C to remove any remaining organic residue to complete the hole transfer process.

To form aluminum pads on the samples, the samples were first vapor-primed with HMDS for ~3 min. Then, PR2020 was spin-coated to a thickness of ~1 μm and soft-baked at 110 °C for 1 min. A light O_2 plasma etch for 1 min was done to remove organic residue from the pattern area prior to metal evaporation. Then, three rectangular pads per membrane area were exposed- one 10 × 10 μm^2 pad in the center plus another two 20 × 20 μm^2 pads at each end of the membrane. Post-

exposure, the resist was baked at 110 °C for 1 min, then developed for 1 min in AZ MIF300 developer. Next, 100 nm of Al was deposited using an Angstrom EvoVac e-beam evaporator at a rate of 2Å/s. Samples were then left to soak overnight in 80 °C NMP to perform liftoff. Post-liftoff, samples were sonicated in NMP, acetone, IPA, and then DI H_2O for 5 minutes each before N2 drying. Finally, a 3 min 70 °C O_2 plasma descum was done to ensure no organic residue remained on the surface.

To define the nanoporous Si membrane shape, the samples were vapor primed with HMDS. Then, PR703 was spin-coated to a thickness of ~1 μm and soft-baked at 95 °C for 1 min. A pair of rectangles was exposed in the location of each device, defining between them a 10×100 μm^2 rectangle with a 10×10 μm^2 Al pad in the center and two 20×20 μm^2 pads at each end. An additional pair of alignment marks was deposited in the Al deposition step, and alignment for this layer was done with those marks to ensure optimal alignment with respect to the Al pads. The lithographic pattern was developed for 1 min in AZ MIF300 developer, then lightly etched for 1 min in O_2 plasma to remove any residue from the pattern area. Next, a Cl_2 plasma was used to etch completely through the silicon to expose in the rectangular areas the underlying SiO_2 of the SOI wafer. After the Si etch, a 3 min 70 °C O_2 etch was used to remove organics formed during the plasma etching process. Then, the photoresist was removed by sonicating the samples in 80 °C NMP and then rinsing with NMP, acetone, IPA, and DI H_2O. At this point, the lithographic portion of the fabrication was complete. Then a vapor-phase HF etch was used to selectively dissolve the underlying SiO_2 and release the membranes from the base substrate in areas where the SiO_2 was exposed in the final lithographic step. A Memsstar VHF Etcher was used, and porous samples were subjected to 1800 s of continuous HF vapor. Control (nonporous) samples required a longer etching time because the lack of pores resulted in less exposed oxide surface area, and were etched

separately for 2600 s. At this point, 10 × 100 μm^2 rectangular membranes with an Al pad in the middle were completely fabricated and suspended from the base substrate and were ready for measurement.

5.2.3. Characterization

In-plane defectivity was assessed via top-down SEM (Carl Zeiss Merlin FE-SEM), while out-of-plane defectivity was inferred from etch-transfer tests into the Si (see Supporting Information for details).

The TDTR system for analysis of κ used two laser diodes (LDs) with wavelengths of 785 and 852 nm. The 852 nm wavelength LD, the pump beam, was electrically modulated to create a quasi-continuous wave with a duration of 4 μs and pulsed every 60 ms to allow for thermal equilibration between pulses[13,22]. The pump beam was used to heat the central Al pad on each device. The 785 nm wavelength LD, the probe beam, was operated in a continuous wave to measure the changes in reflectivity (ΔR) of the central Al pad as its temperature changed. The pump and probe beams were each coupled to a separate optical fiber, which were then attached to a fiber combiner with a single fiber output, and were then perfectly aligned by a collimator before irradiating the sample. The merged pump/probe beam was focused onto the central Al pad of each nanoporous Si device. The spot size of the combined beams was fixed at ~4 μm using an objective lens at 10x magnification, and the beam position was adjusted by monitoring the reflected beam profile using an infrared viewer. The power of the pump and probe beams were set at 50 μW and 1 mW, respectively, to ensure the temperature change (ΔT) of the Al pad remained lower than 10 K. A balance photo-detector coupled with a digital oscilloscope was used to measure the power of the probe beam reflected by the Al pad. Each sample was measured 3 times and 4 identical samples per condition were measured for a total of 12 measurements per sample condition. All

measurements were carried out at room temperature, and the standard error for each measurement was less than 3%. The method used for standard error computation is described in Supplementary Note 5.6.

5.3. Results

5.3.1. Silicon phononic crystal membrane construction

Both SA and DSA samples were fabricated on 45 x 45 mm^2 SOI chips for subsequent analysis of κ_{eff}. The steps required to make a chemical template for DSA made the overall fabrication procedure for DSA structures more complicated than for SA structures, as illustrated in Figure 5.1. The DSA chemical template was prepared as before[13,25], and consisted of a thin film of 67S neutral mat containing a hexagonal array of PS-OH spots with L_S equal to 2 × the p of the BCP. Once the chemical template was created, C2050 BCP was spin-coated and annealed with the same conditions for SA and DSA[13,25]. DSA of the C2050 cylindrical morphology yielded four-fold feature density multiplication relative to the template[28]. This process allowed us to obtain a p of 37.5 nm using an EB-written pattern within the tool's resolution limit.

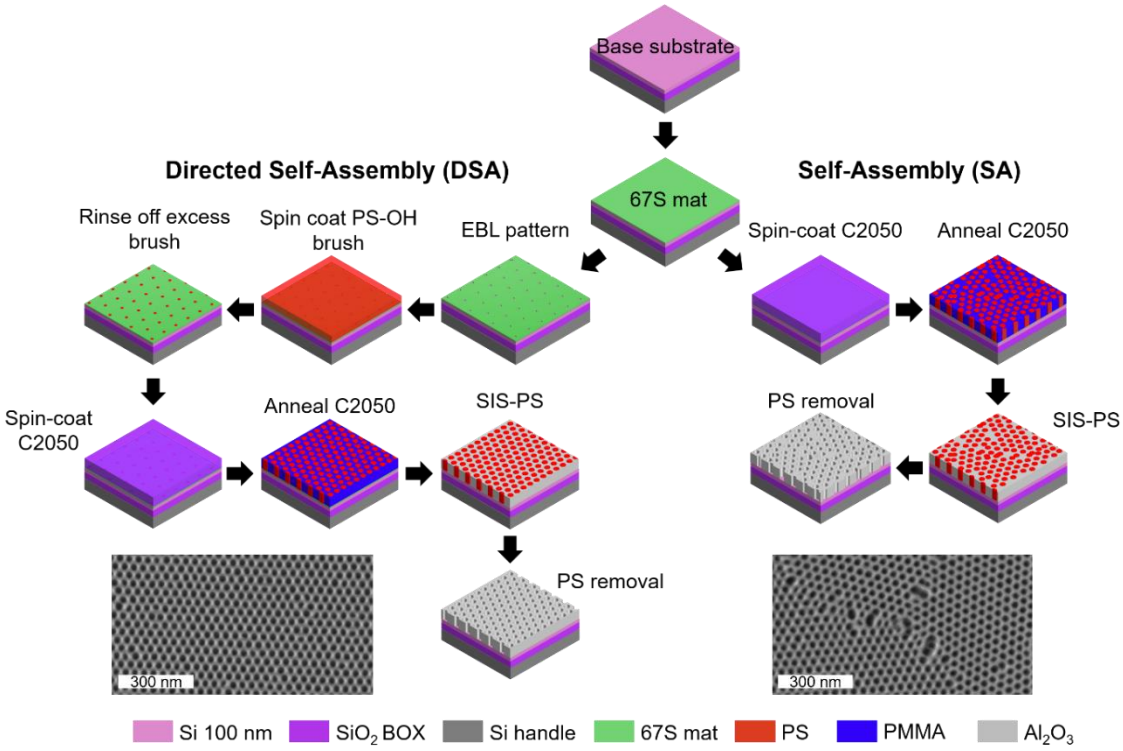


Figure 5.1. Nanoporous template fabrication routes by directed self-assembly (DSA) and self-assembly (SA) of cylinder-forming block copolymer C2050. For DSA, electron beam lithography (EBL) was used to define the initial pattern in the nonpreferential random copolymer mat, 67S. Hydroxy-terminated polystyrene (PS-OH) was grafted into the openings defined in the 67S mat by EBL. Coating and annealing C2050 on the substrates leads to DSA or SA cylindrical PS domains in the C2050. Sequential infiltration synthesis (SIS) is used to convert the C2050 matrix around the PS cylinders into a rigid inorganic hard mask prior to etch transfer. Removal of the PS by a plasma etch forms the dark holes observable in the scanning electron micrographs at the bottom.

The subsequent SIS process converted the organic nanostructure, which is of limited utility as an etch mask, into a mask with etch contrast suitable for transferring the structure deep into a technologically useful substrate like Si. Using SIS determined the upper thickness limit for the 67S mat needed to obtain perpendicular assembly. BCP assembly can tolerate tens of nm of variation in mat thickness, but the thickness window useful for pattern transfer is subject to two constraints: (1) the mat must be thick enough to completely cover the surface and prevent the BCP film from directly interacting with the base substrate, and (2) the mat must not be too thick due to complications with SIS. The mat contained both PS and PMMA, the latter of which accumulated

AlO_x regardless of whether it was in the BCP film or the neutral mat. The thicker the mat, the thicker the underlying "crust" of AlO_x would become. When the mat was too thick (> ~15 nm), the AlO_x accretion in the underlying neutral mat could become difficult to consistently break through with plasma etching, which would cause uniformity issues during etch-transfer into Si. Experimentally, we found the ideal thickness range for the 67S mat was 5–10 nm, post-annealing.

Once the BCP layer was prepared, fabrication of the PnC Si devices could proceed, as illustrated in figure 2. First, we used lithography to pattern the SIS-PS structure so that we could define specific areas for hole transfer into the substrate. This additional lithography step eliminated the risk of unwanted holes or pits being etched into the surface mentioned in Chapter 3, and improved the measurement accuracy of control structures that were intended to remain nonporous. The lithography defined $100 \times 150\ \mu m^2$ areas in the underlying SIS-PS structure where etching would occur. Then an O_2 plasma was used to remove the PS cylinders from the exposed sample area, leaving a nanoporous AlO_x template behind. This nanoporous structure was then immediately used as an etch mask, and a Cl_2/O_2 plasma was used to etch-transfer the holes in the template completely through the underlying Si. Subsequent etches removed the SIS layer and organic residue to complete the pattern transfer process.

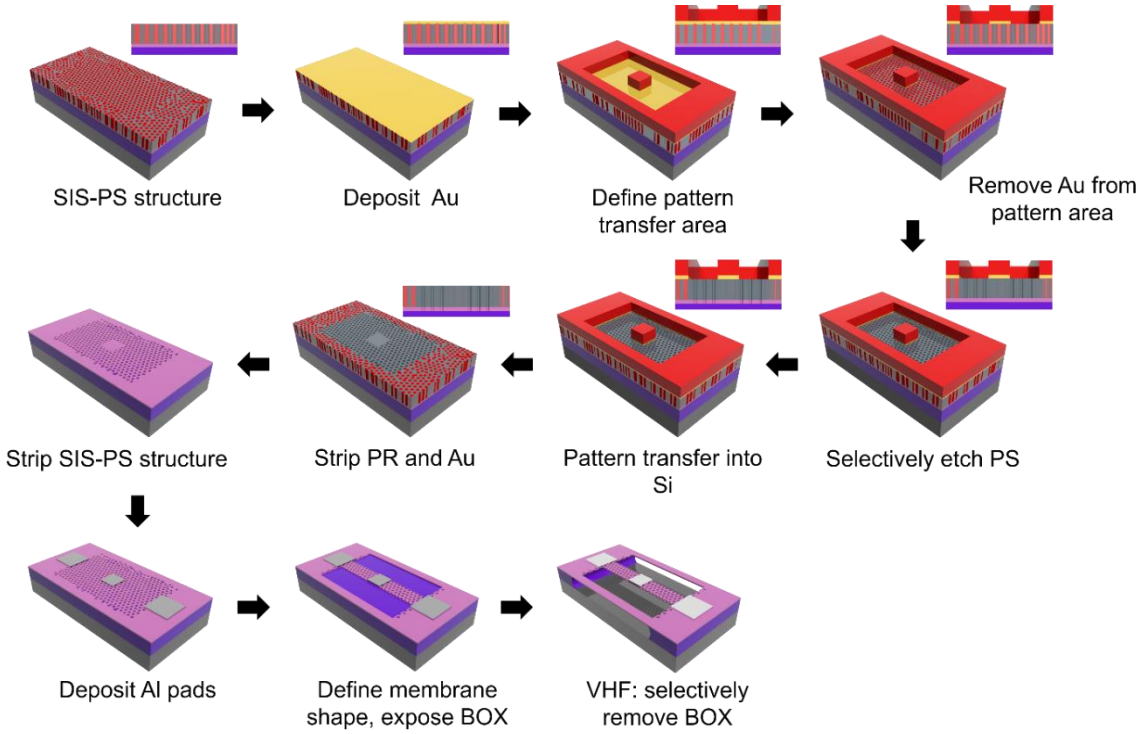


Figure 5.2. Post-SIS fabrication process schematic for forming nanoporous suspended Si structures. The SIS-PS film schematic shows that perfect assembly only occurs where the DSA pattern was made (center), and self-assembled structures were present outside of this area (figure S3). A 20 nm protective Au film was deposited via e-beam evaporation. Photoresist (PR) was patterned to define the area where holes would be etched into Si. Au was selectively removed from the pattern area to expose the SIS-PS film. PS cylinders were selectively O_2 plasma etched from the pattern area. A Cl_2 plasma was used to etch transfer holes from the AlO_x nanostructure into the underlying Si. The Au and PR were stripped, leaving the SIS structure. Note that PS cylinders were only removed in areas where holes were desired in the underlying film. The SIS structure and residual PS were removed, leaving a porous area. A nonporous area remained in the center. Three Al pads were deposited via e-beam evaporation and liftoff, enabling the time-domain thermoreflectance (TDTR) measurement. Photolithography and etching were used to define the shape of the membrane and expose the underlying SiO_2. Vapour-phase hydrofluoric (HF) acid etching was used to selectively remove the oxide beneath the membrane and suspend it fully from the underlying substrate.

It was necessary to (1) add aluminum pads to the membranes and (2) thermally isolate the membranes from the underlying substrate for the TDTR measurements. To form the aluminum pads, which function as heat sinks and the reflective surface used in TDTR measurements, 100 nm of aluminum was evaporated onto lithographically defined areas on the Si structure. Subsequent

liftoff and cleaning resulted in three rectangular pads per membrane area, one 10×10 μm^2 pad in the center plus another two 20×20 μm^2 pads at each end of the membrane.

The Si around the edges of the membrane was then completely removed by a Cl_2 plasma, exposing the underlying SiO_2 of the SOI wafer. A vapour-phase HF etch selectively dissolved the underlying SiO_2 and released the membranes from the base substrate in areas where the SiO_2 was exposed in the preceding lithographic step. At this point, 10×100 μm^2 rectangular membranes with an Al pad in the middle were completely fabricated, released from the base substrate, and ready for measurement. The completed devices are shown in Figure 5.3.

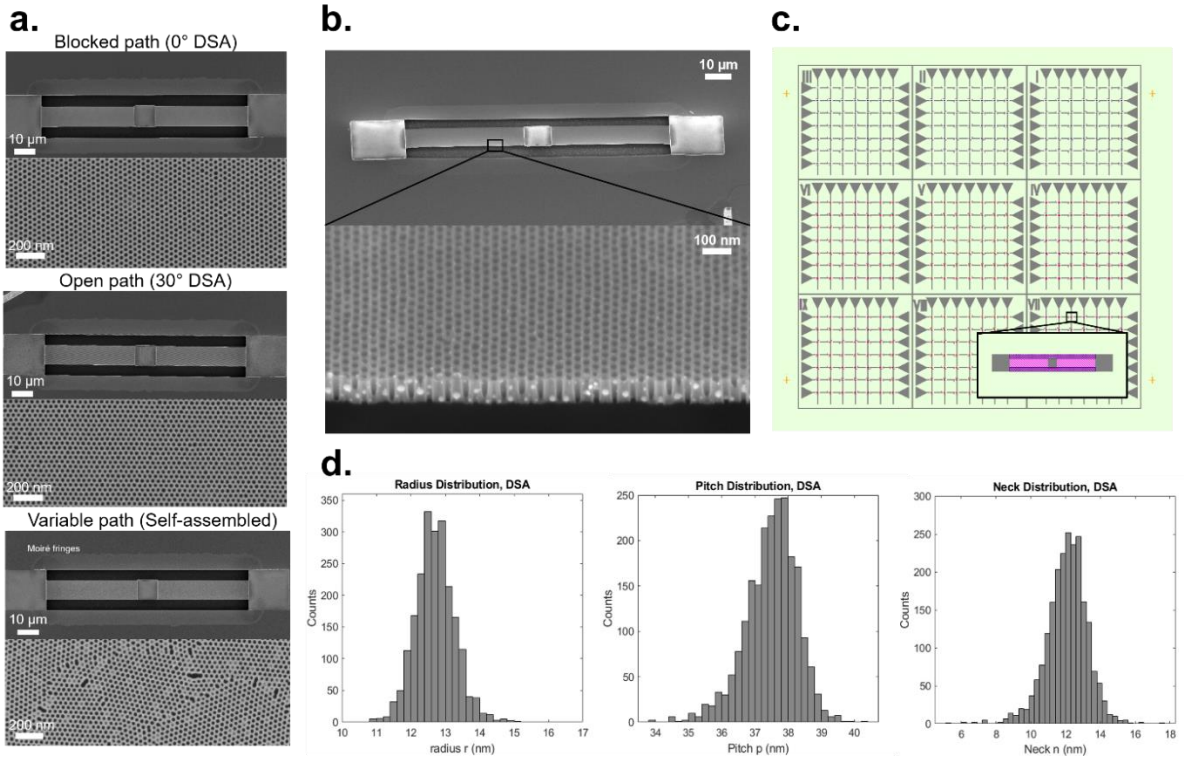


Figure 5.3. SEM Micrographs and dimensions of suspended nanoporous silicon membranes. a) Top-down SEM micrographs of blocked (0° DSA), open (30° DSA), and random path nanostructure configurations formed by block copolymer self-assembly. b) Tilted SEM micrograph of a 0° DSA membrane. From this viewing angle, it is possible to see that the length of the bridge was completely suspended. The magnified image on the bottom shows a highly regular pore profile through the thickness of the silicon. c) A design file showing how many bridges are fabricated per chip, demonstrating how many identical devices can be created simultaneously. d) Histograms showing the size distribution of pitch, neck width, and radius for the DSA structures, plus a table showing the average values of pitch, neck, and radius for DSA

Figure 5.3, continued:
and SA structures. The error was the standard deviation of each dataset. Analysis for DSA dimensions was based on 2177 points for DSA and 13310 points for SA. Only "normal" holes (excluding defect holes at grain boundaries) were considered for the hole, neck, and radius analysis for self-assembled structures. Details about this calculation are available in the SI.

Our work distinguishes itself from the existing studies on sub-100 nm Si nanostructures by combining the defect-free, high precision attributes of EBL (Anufriev, etc.) with the large surface area, minute *n*, and large *P* enabled by BCP DSA. The result are defect-free arrays of HCP holes, with p = 37.5 nm, that extend for hundreds of microns, all with identical average physical characteristics. Tens of identical devices per design, totaling hundreds per chip when considering multiple designs, are fabricated simultaneously. This allows us to precisely compare different pattern orientations across all membranes. To the best of our knowledge, our samples are the most uniform and defect-free samples fabricated at this scale in the literature.

5.3.2. Time-domain thermoreflectance measurements

TDTR was used for determining κ_{eff} of the nanoporous membranes as in our previous work[13,22]. Figure 5.4 shows a schematic of the measurement apparatus, which was based on a two-color pump-probe laser setup. The pump beam heated the central Al pad of the Si membrane with a 4-μs-long quasi-continuous wave that was pulsed every 60 ms to allow for thermal equilibration between pulses. The probe beam was operated in a continuous wave to measure the changes in reflectivity (ΔR) of the central Al pad as its temperature changed.

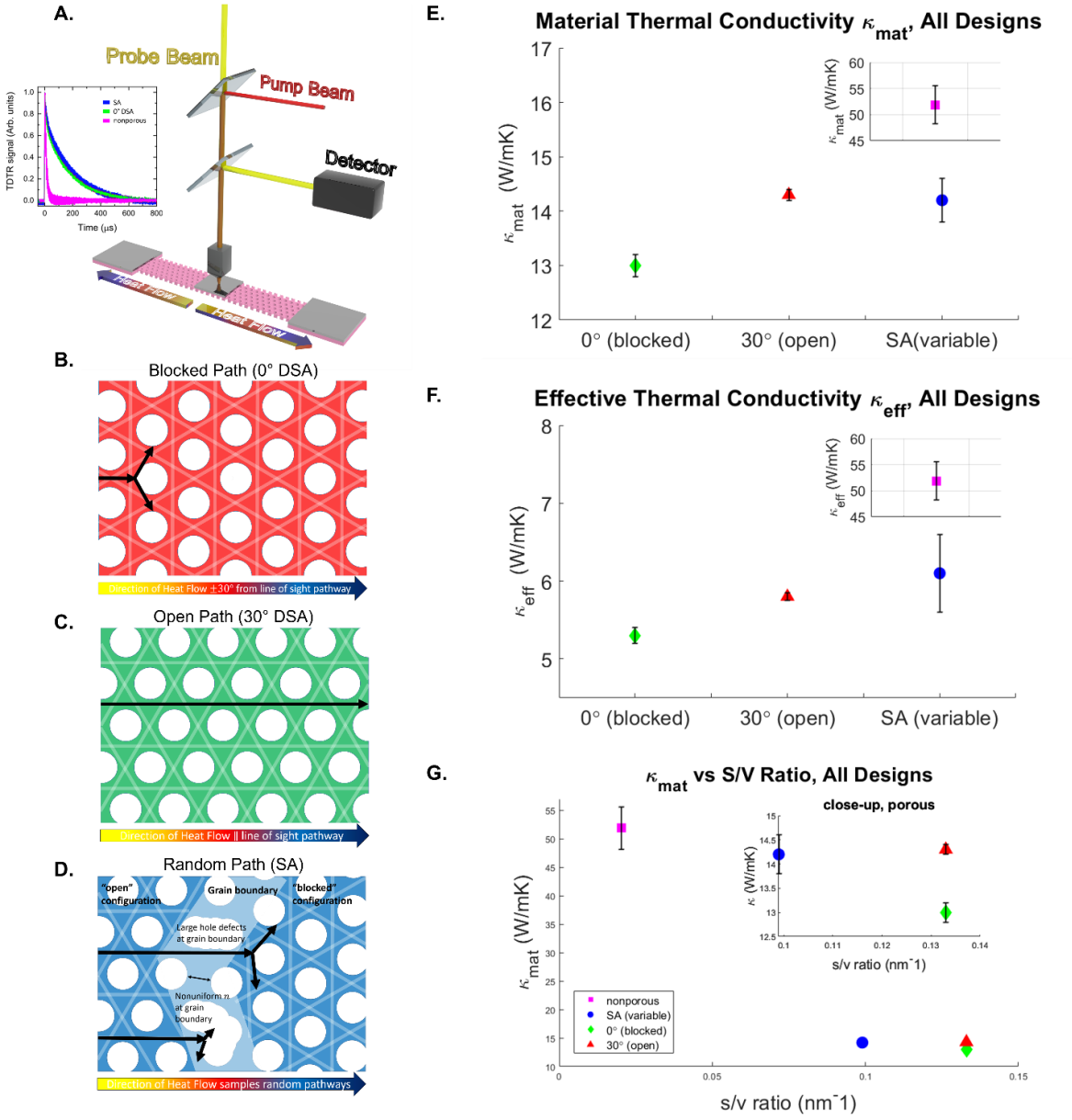


Figure 5.4. Time-domain thermoreflectance (TDTR) measurement results and geometries of membranes. A) Schematic of the TDTR measurement setup, with heat flow and raw signals included. B-D) Illustration of the geometries for open, blocked, and random phonon pathways corresponding to patterns formed from 30° DSA, 0° DSA, and SA of the BCP respectively. Line-of-sight (LOS) pathways through the hexagonal lattice are indicated with light lines. The direction of heat flow is parallel to a LOS path through the HCP lattice for 30° DSA, but is 30° offset from the direction of heat flow for 0° DSA. The black arrows are shown to suggest possible paths for phonons in each sample. Due to the random orientation of grains in the self-assembled geometry, the direction of heat flow samples randomly oriented pathways, plus large neck and hole defects at the grain boundaries. E-F) Material (κ_{mat}) and effective thermal conductivity (κ_{eff}), respectively, for hole geometries made by self-assembly (SA) and directed self-assembly (DSA) structures oriented at 0° and 30° to the direction of heat flow. G) κ_{mat} plotted as a function of surface to

Figure 5.4, continued:
volume (*s*/*v*) ratio for all geometries. The external surface area of the membrane as well as the surface area provided by the pores are included in the determination of *s/v*. The inset shows a close-up zoom of the values for porous samples only.

The TDTR measurements were conducted in a vacuum chamber with a pressure of 5×10^{-4} Pa to prevent convective thermal dissipation. This allowed us to assume that thermal dissipation from the central Al pad occurred predominantly via conduction through the nanoporous Si membrane, implying that changes in the Al reflectivity were solely determined by the thermal properties of the nanoporous Si membrane. As a result, the thermal properties of the Si membrane could be determined by monitoring ΔT of the Al pad after heating by the pump laser. Given a thermoreflectance coefficient β and Al reflectivity R, the change in R can be written as $\Delta R = \beta R \Delta T$. As long as β is assumed constant in the temperature range of the measurement, ΔR should change linearly with ΔT. The inset in figure 4a shows an example of the raw ΔR vs. ΔT. A sum of two decaying exponential equations was used to best fit the changes in R over time t:

$$R(t) = A_1 \exp\left(-\frac{t-t_0}{\tau_1}\right) + A_2 \exp\left(-\frac{t-t_0}{\tau_2}\right) + y_0 \qquad (5.1)$$

where the τ_1 and τ_2 represented transient decay times, t_0 represented the starting time, and the amplitudes A_1 and A_2 were fitting parameters.

The relationship between thermal conductivity κ_{mat} of the Si in the nanoporous structure and the transient decay times τ_1 and τ_2 was determined via a finite element method (FEM) simulation in ANSYS software. The FEM simulations used the same nanoporous geometry as in the Si membrane, and determined the transient decay times for a range of values of the solid matrix in the nanoporous model (κ_{sim}). It was necessary to simulate the same nanoporous structure, as opposed to a simpler, nonporous structure, to more closely match the heat capacity of the nanoporous structure because the heat capacity is required for the modeling the thermal transients

that TDTR measures. Typical ranges for the simulation decay times τ_{1sim} and τ_{2sim} across the various simulations were 100–600 and 5–20 μs, respectively, and were proportional to $1/\kappa_{sim}$. A_1 and A_2 did not appear to significantly change with κ_{sim}. For the determination of $\kappa_{mat,}$ τ_1 was used because it was the larger of the two decay times and therefore more representative of the heat transport along the nanoporous Si structure. To find κ_{mat}, the simulation value of τ_{1sim} was found that most closely matched τ_1 determined from the fit of equation 1 to the experimental TDTR curve. This τ_{1sim} value corresponded to a specific κ_{sim} value, which was determined to be the value of κ_{mat} of the Si in the nanoporous structure of the experimental sample.

It is important to note that the FEM model used Fourier's Law, which only accounts for phonon scattering effects on κ and not the volume reduction effects caused by introducing a nanostructure. Thus, κ_{mat} describes reduction in thermal conductivity solely as a function of phonon scattering. As a result, $\kappa_{mat} \leq \kappa_{Si}$, the thermal conductivity of a nonporous piece of Si with the same dimensions as the Si membrane. From a technological applications point of view, it is also important to know the absolute thermal conductivity of the entire nanoporous membrane, referred to as the effective thermal conductivity, κ_{eff}. To obtain κ_{eff}, the thermal conductivity reduction caused by material volume reduction is derived from κ_{mat} by applying an effective medium model. The Maxwell-Garnett model was used to calculate κ_{eff} based on κ_{mat} and P:

$$\kappa_{\text{eff}} = \kappa_{\text{matrix}} \frac{(1-P)}{(1+P)} \tag{5.2}$$

In previous work with nanoporous SiN_x membranes, the Maxwell-Garnett model matched well with the results of more complicated FEM models[13,22].

Measurement results from TDTR for suspended nanoporous membranes with varying pattern orientations are shown in figure 5.4 and table 5.1. The standard error was calculated for

τ_1, κ_{matrix}, and κ_{eff} based on 12 measurements per sample. The κ_{Si} of the nonporous control bridges was 51.9 ± 3.7 W/mK, which matched values reported for 100 nm thick Si films, giving us confidence that our measurements were accurate[29].

	τ_1 (μs)	κ_{matrix} (W/mK)	κ_{eff} (W/mK)	s/v (nm^{-1})	P	p (nm)	n (nm)
Nonporous	47.2 ± 3.1	51.9 ± 3.7	51.9 ± 3.7	0.020	0.00	-	-
SA	304.7 ± 8.7	14.2 ± 0.4	6.1 ± 0.5	0.099	0.40	37.1 ± 1.3	12.3 ± 2.0
30° (open)	314.5 ± 2.6	14.3 ± 0.1	5.8 ± 0.05	0.133	0.42	37.5 ± 0.8	12.1 ± 1.2
0° (blocked)	348.2 ± 3.9	13.0 ± 0.02	5.3 ± 0.1	0.133	0.42	37.5 ± 0.8	12.1 ± 1.2

Table 5.1. Measurements of decay time τ_1, material and effective thermal conduct00ivity κ_{Si} and κ_{eff}, and the corresponding surface to volume (s/v) ratios. Error for τ_1, κ_{matrix}, and κ_{eff} is the standard error. Error for p and n is the standard deviation.

5.4. Molecular dynamics simulations

To understand the mechanism for the unusually low κ of nanoporous thin films reported experimentally, we carried out molecular dynamics (MD) simulations of κ_{eff} of Si membranes using the GK method and empirical potentials. Previous theoretical work suggests that disorder at the surfaces of the pores may play an important role in reducing the group velocity, the mean free paths and the lifetimes of phonons, thus reducing κ, similarly for nanowires with disordered surfaces [30–32]. Illustrations of our simulated vs. experimental samples are shown in Figure 5.5.

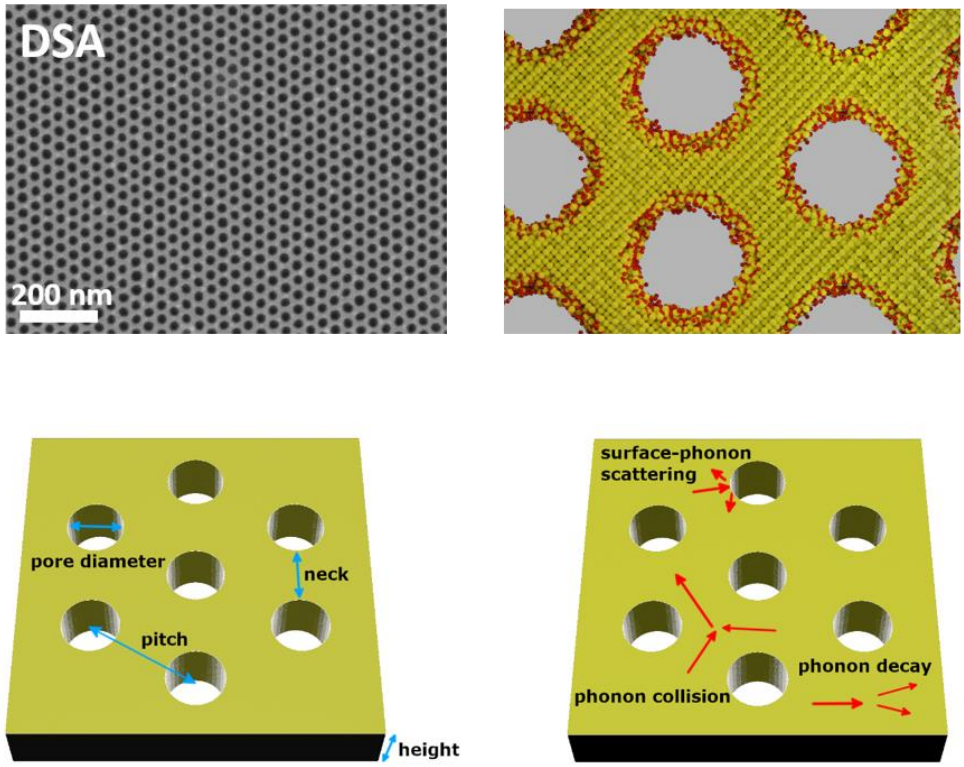


Figure 5.5: Illustrations of the geometry used for molecular dynamics simulations. At the top, a comparison is shown between the experimentally fabricated blocked 0° DSA structure (top left) and the atomistic simulation box (top right). The simulated yellow and red atoms represent silicon and oxygen, respectively. At the bottom left, nomenclature used to describe the geometrical properties of the samples are shown (not to scale). At the bottom right, a schematic representation of the main phonon scattering processes in a nanoporous silicon membrane is shown.

Previous computational works have been limited to structures with dimensions on the order of a few nanometers. In these nanostructures, phonons frequently interact with the boundaries (i.e. the surface of the pores), and phonon-surface scattering processes strongly reduce heat conduction. Generally speaking, when the phonon wavelength is smaller than the surface roughness, the phonon loses coherence and scatters diffusely. When this is the dominant scattering process, the thermal conductivity can be shown to be inversely proportional to the s/v and approximately proportional to the limiting dimension of the structure (i.e. n)[11].

Here, we have studied the room temperature thermal conductivity of Silicon thin films with two-dimensional hexagonal lattice of pores with periods between 7.5 and 37.5 nm and porosity

between 20% and 40%. The porosity is in the range that is typical for the BCP DSA nanolithography technique described in the experimental section, and the range of periods nicely bridge the gap between previously available MD results and available experimental studies.

All simulations were performed using LAMMPS and the Tersoff potential, previously used to study thermal properties of nanowires in the presence of oxidation[30,33,34]. To understand the effect of oxidation on the thermal conductivity of porous Si bridges we compared systems containing only Si and samples in which the surface of the pores was oxidized.

The non-oxidized samples were prepared by carving the pores from a crystalline sample of pure Si to obtain the desired pitch and pore diameter, followed by a coordinate minimization and a short equilibration to let the Si surface reconstruct. The samples with oxidized pore surfaces were created by removing a Si annulus with a width of 0.5 nm of Silicon from the interior surface of the pore and substituting it with a layer of amorphous SiO_2 of the same volume, in order to keep the porosity and the pitch of the system unchanged. The amorphous layer was obtained from a bulk amorphous SiO_2 prepared by melting crystalline SiO_2 at 5300K, followed by annealing at a cooling rate of 1.6 K/ps. The sample was kept at a pressure of 1 atm during the annealing, resulting in a final density of 2.25 g/cm^3, close to the experimental density of amorphous silica. After the addition of the amorphous layer to the pure Silicon matrix, the whole system was kept at 900K for 1 ns and slowly cooled to 300K to let the exposed surface of the amorphous layer relax and the amorphous SiO_2 layer adhere to the Silicon lattice.

The thermal conductivity was calculated using the Green-Kubo method. Since it is not possible to simulate bridges of 100 nm thickness, we used periodic boundary conditions and normalized the thermal conductivity by the ratio of the bulk thermal conductivity and the thermal conductivity of a non-porous silicon bridge 100 nm thick. In the case of pristine porous silicon

bridges, we calculated the heat current autocorrelation function with a timestep of 1 fs, a sampling rate of 2 fs for 10 n using 8 replicas, for a total of 80 ns at each combination of pitch and porosity. In the case of oxidized porous silicon, we used a timestep of 0.2 fs, a sampling rate of 1 fs for 5 n using 10 replicas, for a total of 50 ns for the 37.5 nm pitch and 16 replicas, for a total of 96 ns at 37.5 pitch.

5.4.1. Molecular dynamics results

In figure 5.6 we present our results for the in-plane thermal conductivity of Si PnC membranes in the absence of oxidation as a function of pitch and porosity compared to *n*, *s/v*, and pore diameter. This material is anisotropic, and we can expect the thermal conductivity in the cross-plane direction to be different from that in the in-plane direction. Indeed, we found that in our simulations the cross-plane thermal conductivity is around twice as large as the one in-plane. Only the in-plane thermal conductivity was measured, so in what follows we limit our discussion to this component. We explored three porosities (20%, 33% and 40%) and three pitch sizes (7.5, 22.5 and 37.5 nm) for a total of nine combinations, to capture the range of experimentally feasible porosities and pitches. For a 40% porosity and a 37.5 nm pitch, we observed a thermal conductivity of 3.3 ± 0.3 W/mK, which is consistent with the thermal conductivity of 4.8-5.3 W/mK at the same pitch and 42% that we measured experimentally for the DSA-patterned membranes.

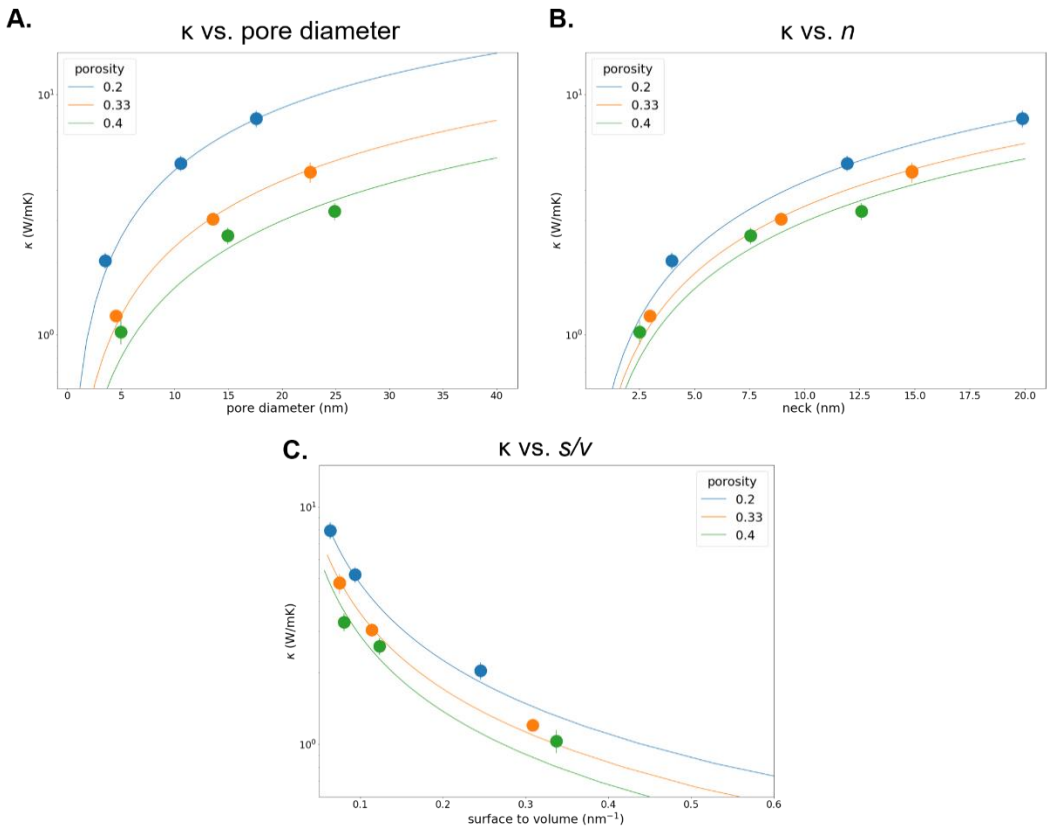


Figure 5.6: Summary of molecular dynamics simulations. (A) Thermal conductivity of nanoporous silicon bridge as a function of the diameter of the pores and porosity. The pore diameter is calculated using Eq 4.1. (B) Thermal conductivity of nanoporous silicon bridge as a function of neck length and porosity. The neck length is calculated using Eq. 4.2. (C) Thermal conductivity of nanoporous silicon bridge as a function of the surface-to-volume and porosity. Solid lines are calculated from a single fit of Eq. 4.3 using all data.

Our results are summarized in Table 5.2. As expected, the thermal conductivity increases with increasing pitch and with decreasing porosity. The pore diameter d_p is:

$$d_p = \frac{\sqrt{2}\sqrt[4]{3}}{\sqrt{\pi}} p\sqrt{P} \tag{5.3}$$

Here d_p is the pore diameter, p is the pitch and P is the porosity. We find that the Prasher model properly fits our data, with the exception of the higher porosity samples, where the thermal conductivity is underestimated at low pitch and overestimated when the pitch is longer than approximately 30 nm. In Figure 5.6 we show our data as a function of the neck size, defined as:

$$n = p - d_p \tag{5.4}$$

Sample	Porosity (%)	Pitch (nm)	κ(W/mK)	δκ
MD	20	7.5	2.0	0.2
MD	20	22.5	5.2	0.4
MD	20	37.5	7.9	0.6
MD	33	7.5	1.20	0.05
MD	33	22.5	3.0	0.1
MD	33	37.5	4.8	0.5
MD	40	7.5	1.0	0.1
MD	40	22.5	2.6	0.2
MD	40	37.5	3.3	0.3
0° DSA (blocked)	42	37.5	5.3	0.1

Table 5.2: Thermal conductivity of porous silicon bridges, 100 nm thick, as a function of porosity and pitch. MD indicates results of the molecular dynamics simulations on blocked configuration nanostructures with varying *p*, *P*, and *n*, while 0° DSA refers to the experimentally fabricated and measured membranes with the blocked (0° DSA) configuration.

We also computed the thermal conductivity of the Si PnC membranes in the presence of surface oxidation. In this case we only studied samples with a 33% porosity so far. We observe a large, approximately 4 fold reduction in the thermal conductivity of the sample with the 7.5 nm pitch, but little to no change in the sample with a 37.5 nm pitch. The large decrease we observed can be justified by observing that (1) the sample with the smaller pitch contains a larger percentage of amorphous silica, compared to Si; (2) the layer of amorphous silica reduces the fraction of the neck composed of pure Si by approx. 40% in the smallest sample, but only by approx. 7% in the 37.5-nm-pitch sample. Amorphous SiO_2 has a much lower thermal conductivity than Si (2.7 and 146 W/mK, respectively), which partly explain the reduction in thermal conductivity after oxidation. Moreover, the addition of the amorphous silica layer increases the amount of phonon scattering at the pore surface, because of the different material and because of the increase in the surface area available for surface-phonon scattering. Finally, we suspect the addition of the amorphous silica layer reduces the group velocity of long-wavelength acoustic phonons, due to the different elastic properties of silica and silicon. Since long-wavelength phonons are important contributors to the overall thermal conductivity, a reduction in their group velocity would greatly

reduce the thermal conductivity. It is reasonable to assume that the reduction in group velocity following oxidation would be more pronounced in the sample with the smaller pitch.

We conclude our discussion of the MD results by comparing them to those of models often adopted in the literature. When the phonon MFPs are comparable to the d_p and p, effective-medium models fail in predicting κ of nanoporous materials. In theory, the BTE, complemented by the Allen-Feldman theory of thermal transport, could be used instead. However, solving the BTE in such a complex network of pores, with such a large elementary cell, is impractical. Monte Carlo ray tracing transmission models, based on an approximate solution of the BTE, overestimate the thermal conductivity of Si PnC membranes once the pitch is smaller than 500 nanometers[12,35].

As an alternative, Prasher proposed an approximate model for predicting the thermal conductivity of phonons in two-dimensional nanoporous materials made from aligned cylindrical pores, which turns out to agree rather well with the results of our MD simulations[36]. The model captures the size effects due to the interplay between phonon MFP, d_p, and p, and reduces to the effective-medium models for macroporous materials. The full derivation of the model can be found in Reference 36. The final equation expresses κ_{eff} of the nanoporous material as a function of two transport properties of the bulk material and two geometric properties of the nanoporous structure: the thermal conductivity κ_0 and the MFP l of the phonons in the original bulk material; and P and d_p in the porous structures:

$$\kappa(P, d_p, l) = \frac{\kappa_0}{\frac{1+P}{1-P} + \frac{1}{q(d_p,P,l)F(P,d_p)}} \tag{5.5}$$

The so called view factor F is given by:

$$F(P, d_p) = 1 - \frac{d_p}{L}\left(\frac{\pi}{2} - \left(\sin^{-1}\frac{d_p}{L} + \sqrt{\left(\frac{L}{d_p}\right)^2 - 1} - \frac{L}{d_p}\right)\right) \tag{5.6}$$

And the rescaled lengths d and L are:

$$q = \frac{3d_p}{8l}\sqrt{\frac{\pi}{P}} \qquad L = d_p\sqrt{\frac{\pi}{4P}}$$

The Prasher model does not take into account the reduction in thermal conductivity due to the finite thickness of the silicon bridge. Other models incorporate this effect, but we found they overestimated the thermal conductivity for large pore diameters and in the limit of zero porosity. Therefore, we used the simpler Prasher model, with κ of a suspended silicon bridge with zero porosity (72 W/mK) in place of the bulk κ. Finally, the Prasher model contains the parameter *l*, the bulk phonon MFP. We used our data to fit *l*, finding *l* = 67.0 ±1 nm.

5.5. Discussion

Because κ_{eff} only adds the volume reduction effects of *P* to κ_{matrix}, we are primarily interested in the parameters that could affect κ_{matrix} in nanostructured Si, such as *n*, *p*, *s*/*v*, and nanostructure configuration, which can affect phonon directionality. We explored three primary nanostructure configurations: blocked pathways (0° DSA), open pathways (30° DSA), and random pathways (SA), as illustrated in Figure 5.4B-D. The blocked configuration refers to the 0° orientation of the HCP array of nanopores relative to the direction of heat flow, as shown in figure 5.4B. In this orientation, there are no line-of-sight pathways parallel to the direction of heat flow. Rather, staggered holes are directly present in this line-of-sight path, resulting in a partially blocked pathway. However, when the hexagonal lattice is rotated 30° with respect to the direction of heat flow, there are open, line-of-sight pathways through the Si nanostructure that are parallel to the direction of heat flow, as shown in Figure 4C. In the polygrained SA structures, a variety of randomly oriented line-of-sight pathways within each grain are present along the direction of heat flow, as illustrated in Figure 5.4D. The value of κ_{mat} for the blocked (0° DSA) pathway samples is 9.5% and 13.1% smaller than the open pathway (30° DSA) and SA structures, respectively. Due to the number of simultaneously fabricated samples that could be measured, as well as the precision

afforded by the TDTR system, we could determine that the difference between the κ_{mat} value for the blocked structure and the κ_{mat} values of the open (30° DSA) and variable path (SA) structures was statistically significant (t-test $p < 0.01$). Comparison of the 0° DSA and 30° DSA configurations is helpful because both samples have identical *P*, *p*, *n*, and *s/v*. We can conclude that the difference in κ_{mat} of the 0° and 30° DSA samples was due to the difference in potential phonon pathways shown in Figure 5.4 for the two configurations. The blocked configuration had the lowest κ_{mat} value, as one might expect.

It was interesting that the open configuration had a lower κ_{mat} value than the SA configuration. The difference in κ_{mat} between the SA and open structures could be due to their substantially different values of *s/v*, which magnify a small difference in *P* between the DSA (42%) and SA (40%) structures. We believe that the complex defect structures at grain boundaries in the SA samples caused this small, but measurable, difference in *P*. While defects, like all other BCP features, are compositionally balanced, defects at grain boundaries are fundamentally three dimensional in nature[37,38]. As etch-transfer is a top-down process and only samples the geometry present at the top of the film, more oversized necks than oversized holes are present at the grain boundaries (Figures 3 and 4) after etch-transfer into Si. As a result, the *P* for DSA structures was slightly smaller than the SA structures, despite all structures having been fabricated under identical conditions simultaneously. The Maxwell-Garnett model (equation 5.2) provides a classical effective medium approximation to account for the loss of material caused by *P* to determine κ_{eff}. The difference in porosity of the SA and DSA systems result in a ~5% change in κ_{eff}. In contrast, the small difference in *P* causes their *s/v* values to differ by ~25% (0.133 nm^{-1} and 0.099 nm^{-1} for DSA and SA configurations, respectively).

In Si, as the proportion of surfaces increases, boundary scattering of phonons increases, and κ_{matrix} decreases[5,8,10,21,24]. While *s/v* does not give any specific information about the specific physical dimensions of a given nanostructure, it is a useful analytic parameter because it enables comparison between different nanostructures as a function of interfacial area regardless of form factor. For example, consider two Si membranes (100 nm × 100 µm × 10 µm) with equal *n*. A sample with p = 1000 nm, r = 495 nm, and P = 88% structure will have $s/v \sim 0.05$, whereas a sample with p = 20 nm, r = 5 nm, and P = 23% has $s/v \sim 0.13$. Even though both structures have identical *n*, the smaller *p* sample has both smaller *P* and larger *s/v*, indicating that it could have larger κ_{matrix}.

The larger κ_{matrix} of the SA configuration compared to the open configuration could also be due to instances of larger necks that can occur in the SA configuration at grain boundaries. While the average *n* of the SA and open configurations were effectively the same, at ~12 nm, the larger error of the *n* measurement of the SA system points to the existence of these larger necks. Larger necks could enable phonon conduction, resulting in a larger overall κ_{eff} than either the blocked or open configurations.

Often for nanostructured PnCs, trends in κ_{matrix} are analyzed and discussed primarily as a function of *n*. As the smallest dimension of the heat conducting material in the nanostructure, *n* defines the maximum space available for phonon travel. From a boundary scattering perspective, scattering increases with decreasing system size. As *n* becomes smaller than the average MFP of the primary heat carriers in a system, phonon scattering increases. This effect has been observed for *n* as large as several micrometers[1,9,21] and documented down to *n* of ~20-40 nm[8,11,14]. For these length scales, the smaller *n* becomes, the larger *s/v* becomes, and the stronger scattering in the nanostructure becomes. This is best illustrated by comparing κ_{mat} to s/v as illustrated in Figure

5.5G, which shows a strong decrease in κ_{mat} as the area of interfaces increases. In this work, the average value of *n* was effectively the same, ~12 nm, for all samples, as shown in figure 3. The large values of *s*/v enabled by small values of *n* are likely main cause of low κ_{mat} values of the porous samples (13–15 mW/K) compared to the κ_{Si} of the nonporous Si membrane (~52 mW/K).

5.5.1 Comments on phononic crystal design

It is worth discussing the application design implications of *p*, *P*, *n*, and *s/v*. Previous works have showed that κ trends strongly with decreasing *n*, with a less pronounced dependence on *p* or *P*[3,9,11,39]. This trend has been demonstrated experimentally for n >≈15, and our results extend this trend down to 2.5 nm. Some authors have even claimed that the thermal conductivity should be only a function of neck size when it is smaller than 100 nm, a distance comparable to the MFPs of phonons in bulk Si[11].

Theoretically, *n* is independent of *p*; that is, a structure in which *p* = 1000 nm with *r* = 495 nm and a structure in which *p* = 20 nm with *r* = 5 nm could both have *n* = 10 nm. However, the *p* = 1000 nm sample would require a *P* of ~88% to achieve such a small neck width, while the *p* = 20 nm sample would only require a *P* of ~23%. The constraints informing which structure one might choose for a PnC design are heavily limited by the capabilities of nanofabrication. Reactive ion plasma etching is a common technique used to etch the holes to create PnCs, but becomes limited when the size of the nanostructure forces the plasma ions into the Knudsen flow regime (for example, in high aspect ratio holes with small d_p). Additionally, plasma etching recipes often have etch rate variation on the order of a few nanometers (as discussed in Chapter 4), which can be heavily tool dependent and can also change over time as the chemical environment inside the plasma chamber evolves with long-term use. While a deviation of a few nanometers is relatively insignificant for nanostructures with *n* > 50 nm, it is extremely significant when *n* < 20 nm, and

can result in collapsed walls between pores, sidewall broadening, and other undesirable processing artifacts.

Mechanical stability and ease of processing are just as important to consider as the theoretical minimum dimensions needed to increase phonon scattering when designing a PNC device for these kinds of thermal experiments. While large *P* is desirable from an intuitive material reduction perspective, large *s/v* becomes increasingly unattainable as *P* increases. Furthermore, a structure with very small *n* at larger *P* tends to be both mechanically unstable and subject to undesirable etching defects, especially for suspended nanostructures, making them impractical design targets. While *p* itself is relatively unimportant from a scattering perspective (at least, for *p* larger than the average wavelength of the heat carriers), small *p* enables small *n* even at small *P*, while large *p* makes small *n* difficult to attain even with a large *P*.

Our simulations and modelling provide additional evidence that thermal conductivity is not solely a function of *n*. In agreement with several existing experimental and computational studies, our results suggest that thermal conductivity most strongly trends with *s/v*, due to the increased phonon scattering at the surface of the pores[3,11,30,39–42]. Overall, from both a design and functional perspective, the most functional and attainable PNCs have a small *p* with *n* comparable to some portion of the MFP spectrum of the phonons. The size of *n* is tunable by *P*, which is much easier to do when the maximum *P* required for the target *n* is small than large. Furthermore, smaller *p* combined with small *n* maximizes the possible values of *s/v*, which is proportional to the amount of phonon boundary scattering in a material.

Thus, while all physical parameters discussed here are critical to PNC design and performance, *p* and *P* are relatively more important from a design perspective, while *n* and *s/v* are critical from a functional and analytical perspective. It could be helpful to think of *n*, *p*, and *P* as

parameters that are cooperatively tuned to design a structure with the highest possible *s/v* while retaining mechanical stability. Beyond that, the presence and orientation of aligned channels with respect to the direction of heat flow are additional factors to consider when designing a low-κ PnC.

5.5.2. Directional phonon transport

Due to the relatively large average MFP of phonons in room temperature Si[43] (~300 nm at 300 K), combined with the typical dimensions for Si nanostructures, ballistic transport through these nanostructures is technically possible. Several studies have both experimentally and computationally examined the geometric configuration of the nanostructure with respect to the direction of heat flow to determine whether κ_{eff} is affected[9,10,24]. There is a growing body of evidence to support the hypothesis that the directionality and angular distribution of phonons in a Si nanostructure can be measurably influenced by the geometry of the nanostructure. Two general types of lattices have been commonly investigated: aligned lattices, where a contiguous pathway through the nanostructure is parallel to the direction of heat flow, and staggered lattices, where staggered holes are present in the path of heat flow, and there is no contiguous open pathway through the nanostructure.

The aligned and staggered lattices are conceptually identical to our open and blocked pathway 30° and 0° DSA samples. Studies on staggered lattices have found evidence of large angular distributions of phonons because the phonons scatter diffusely at the holes present in the heat flow pathway, which both reduces the velocity of the phonons, thereby reducing κ, and prevents them from developing directionality[9,19,24,30]. For aligned lattices, the same studies show a narrow angular distribution of phonons, implying that aligned lattices allow phonons to acquire some degree of directionality and travel partially ballistically through those lattices, resulting in larger κ_{mat}[9]. This could be due in part to phonons with large MFP in room temperature Si scattering

tangentially from hole walls defining each aligned channel, enabling a gradual accumulation of phonons travelling ballistically. Anufriev et. al. found evidence supporting that aligned lattices, when capped with a Si nanowire, can indeed serve as sources of directional, ballistic phonons in the nanowires[9]. Their experimental results also strongly support that the directionality effects of Si nanostructures on heat transport become increasingly prominent as minimum dimension is reduced below 30 nm. We believe that our experiments probing the effects of nanostructure directionality on thermal conductivity are not only in agreement with previous work, but also expand understanding to the 10–15 nm regime.

Broadly, mechanistic explanations fall into two categories: (1) coherent wave scattering and (2) incoherent, diffuse, interfacial scattering. For coherent scattering, the nanostructure, the underlying lattice, or both, would interfere with phonons and potentially specularly reflect phonons out of the nanostructure. For incoherent scattering, phonons scatter diffusely at surfaces, interfaces, and defects, which reduces the population of phonons moving on a direct path through a material, thereby lowering its κ_{eff} . While some studies on Si nanostructures report observations of coherent wave scattering of phonons[8,21,44], many studies suggest that such contributions to phonon scattering are only meaningful at very low T (< 10 K), with negligible contributions at room temperature[7,11,45,46]. This difference in behavior at very low T is attributed to surface roughness in the nanostructures that destroys coherence at temperatures where the roughness is comparable to or larger than the dominant phonon wavelengths[19,20,32,47,48]. Roughness of a Si nanostructure is typically at least a few nanometers, and often significantly larger depending on the process type/quality, as well as atomic-scale disorder at the hole edges[30]. In this work, given that our devices were measured at room temperature, we believe that diffuse, boundary scattering accounts for the strong reduction in κ_{mat} (and κ_{eff}) observed. The difference in κ_{mat} between different device

geometries were a result of different amounts of phonon scattering based on the nanostructure orientation, and in the case of κ_{eff} of the SA membranes, slightly larger *P* and *s/v*.

On a broader level, although we measure statistically significant differences in κ_{eff} between the open and blocked configurations, the 4.1 %, or 0.3 W/mK, difference in κ_{eff} between SA and open configuration at room temperature was not statistically significant. This tells us that the polycrystalline hole structure of the SA membranes is approximately functionally equivalent (at least in terms of absolute magnitude of κ_{eff}) to having aligned channels parallel to the direction of heat flow. As the fabrication process for DSA samples is much more time- and resource-expensive than the fabrication process for SA films, SA structures could be a robust and relatively easy method for fabricating high *s*/*v* ratio nanostructures with very small pitch and neck. However, we believe that if the objective of a PnC experiment is to create channels of high energy flux enabled by ballistic transport, there would likely be functional differences between the two structures despite having overall similar values of κ_{eff}.

The differences between SA and blocked structures were more significant: we measured a 13.2%, or 0.8 W/mK, difference between SA and 0° DSA at room temperature. Thus, for the lowest possible κ_{eff} in a room temperature application, a staggered or blocked structure is the most effective design target, and going through the labor of DSA to achieve such a structure is both meaningful and effective. While 0.8 W/mK is still a relatively small difference given that all nanoporous structures in this work had κ_{eff} reduced at least 88% relative to the nonporous control structures, it is important to remember that these measurements were only conducted at room temperature. Previous work has shown that coherent scattering contributions become more significant with at decreasing temperatures, as cold phonons have lower energies, longer wavelengths, and longer MFPs. It has been reported by Anufriev et al. that differences in κ_{eff}

between staggered and aligned lattices with n of 60 nm could diverge more strongly with decreasing T as well[7,11]. While low-T measurements were beyond the scope of this work, we believe that our device design is an excellent candidate for probing fundamental questions of phonon transport at length scales on the order of 10 nm, which has yet to be done in existing literature.

Ultimately, all three geometries have similar p, n, s/v, and P, with measurable differences in τ_1, κ_{mat}, and κ_{eff} likely emerging due to differences in phonon transport and scattering in each of the geometries. We believe that our fabrication process could be easily tailored to a variety of cylinder forming block copolymers of smaller or larger pitches as well, making it a robust and customizable methodology for fabricating large area, high uniformity silicon nanostructures with narrow feature distributions that function as low-κ phononic thermocrystals.

5.6. Conclusions

Similarly to other work[9–11,13,18,14], we believe that the bulk of the reduction in κ_{eff} in our devices is the result of strong diffuse phonon scattering at surfaces and interfaces. Previous theoretical and experimental studies in larger (n > 100) Si nanostructures at room temperature support the concept that open pathways aligned with the direction of heat flow encourage directional alignment of phonons, resulting in ballistic transport along those pathways. Similarly, these studies found evidence that the presence of staggered pores in the direction of heat flow scatter phonons and prevent directional, ballistic transport, resulting in smaller κ_{eff}. Our results here agree with previous work, and imply that the dominant mechanism in κ_{eff} reduction at room temperature is strong phonon scattering at interfaces. Differences in the measured value of κ_{eff} between different nanostructure geometries was a result of differing amounts of diffuse scattering based on n, s/v, and the openness of the pathway parallel to the direction of heat flow.

Our simulations provided a microscopic understanding of thermal transport in np-Si materials, the relation between morphology and thermal conductivity, including the effect of porous oxidation at smaller pitch. We found that our simulation results are correctly fitted by the Prasher model, which we hope will assist in engineering of the thermal conductivity of these and similar devices.

In sum, our experimental and simulation results were in agreement with previous literature regarding both magnitude of κ reduction and the likely mechanisms. We further conclude that for our devices with *n* on the order of 10 nm, the reduction in κ_{mat} and κ_{eff} by diffuse scattering trends with both *s/v* and the presence of aligned channels parallel to the direction of heat flow. Our results demonstrate that for nanostructures with a minimum dimension on the order of 10 nm, sample geometry has a measurably significant effect on κ_{mat} and κ_{eff}, even at room temperature, likely as a result of modifying the directionality of phonon transport within aligned nanostructures.

5.6.1 Acknowledgements

We gratefully acknowledge financial support from the Panasonic Corporation. This work made use of the Pritzker Nanofabrication Facility (PNF) of the Pritzker School of Molecular Engineering at the University of Chicago, which receives support from Soft and Hybrid Nanotechnology Experimental (SHyNE) Resource (NSF ECCS-1542205), a node of the National Science Foundation's National Nanotechnology Coordinated Infrastructure. This work also made use of the shared facilities at the University of Chicago Materials Research Science and Engineering Center, supported by National Science Foundation under award number DMR-2011854. The authors thank the PNF staff and Peter J. Duda III for their support, and Masaki Fujikane for insightful discussions.

5.7 Supplemental Information

5.7.1 Neutral mat synthesis

The neutral mat used to create an energetically neutral surface to both poly(styrene) and poly(methylmethacrylate) was a random copolymer synthesized via RAFT. Styrene and methyl methacrylate monomers were mixed with glycidyl methacrylate, and AIBN was used as the initiator. Styrene compositions of 0.4-0.6 were targeted, and styrene compositions of 0.45-0.68 were obtained. Composition was verified by proton NMR. The mat best for perpendicular assembly of PS(20k)-b-PMMA(50k) cylinders was found to be 67% styrene, designated 67S.

5.7.2 Etch-transfer characteristics and film defectivity

Three of the neutral mats we synthesized- 6, 7, and 8 corresponding to 60S, 63S, and 67S- yielded high quality assembly as seen in top-down SEM. However, it is known in BCP literature that the surface is not necessarily a good indicator of whether defects are present in the thickness of the film or at the bottom interface. Since the BCP in this work is used for pattern transfer into an underlying substrate, we determined that the most sensible way to test whether the BCP film would pattern transfer well (for each neutral mat condition) was to do the pattern transfer and evaluate the quality of the transferred hole pattern.

BCP was assembled on top of each of the 3 different mats and subjected to SIS and PS cylinder removal as illustrated in Figs. 1 and 3. Then, the samples were etched in Cl_2 plasma for 1 minute to etch transfer the holes into the Si. The nanoporous Al_2O_3 SIS structure and the post-etch porous Si were analyzed to determine pattern transfer quality for each mat. Mat 60S had large parallel defects, small grains, and many large defects at grain boundaries. Mat 63S lacked the large parallel defects, but had small defective grains as well as lots of large defects at the grain boundaries. Relative to 60S and 63S, 67S had the largest grains and smallest defects at the grain

boundaries. By this method, we selected mat 67S as the mat leading to the highest quality etch-transfer quality (Figure 5.5).

It would be difficult to assess film quality more rigorously, as that would require doing hours of TEM and would be both impractical and expensive to do. This is a relatively fast way to assess film quality in a way that is helpful for establishing our process windows.

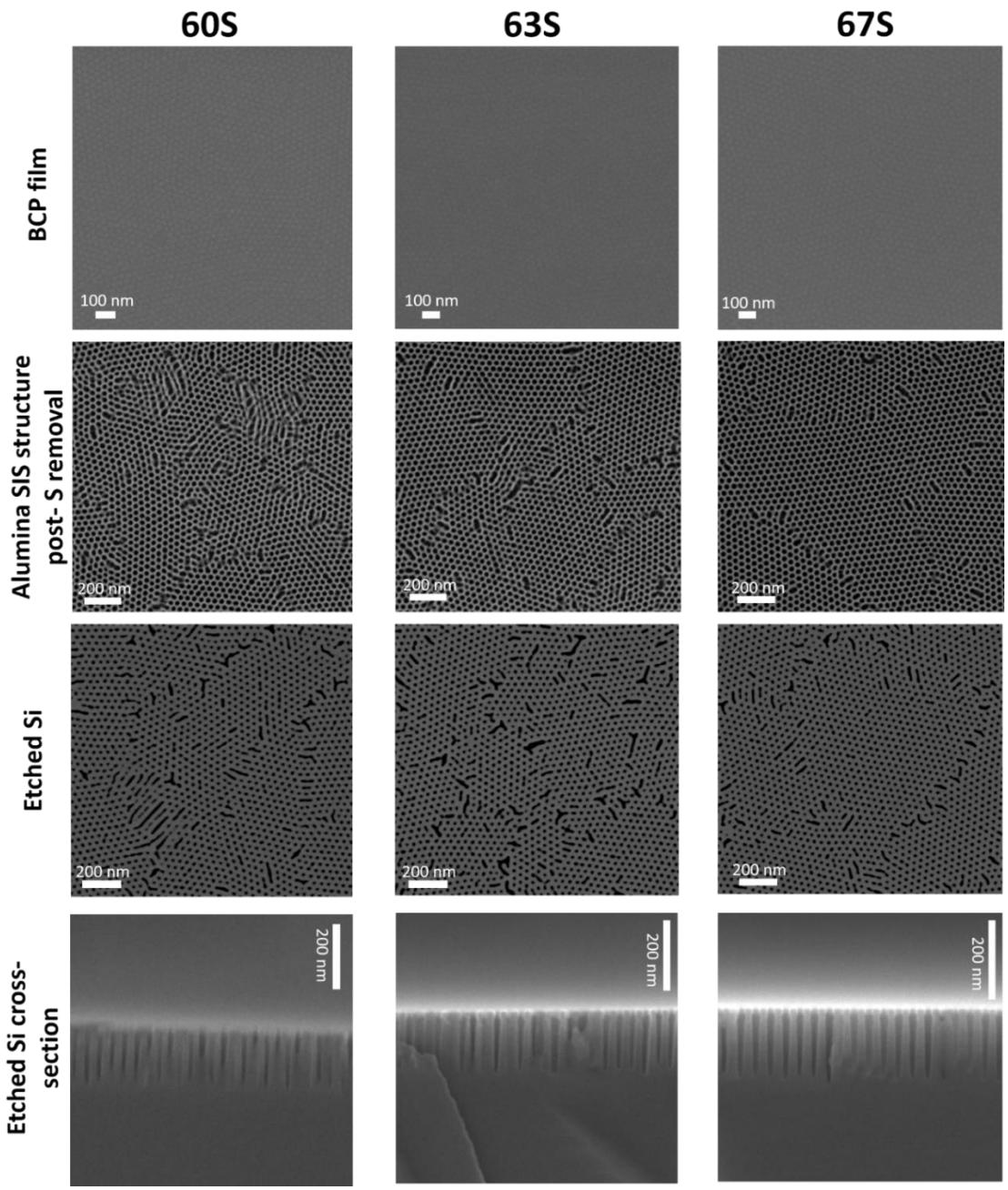


Figure 5.7 Images of C2050 assembly and pattern transfer on three different neutral mats synthesized for this work. Differences in BCP film quality in self-assembled applications showed very little difference. Top row shows the BCP film as-annealed; bottom row shows the same films after sequential infiltration synthesis (SIS) to convert the PMMA domain into AlO_x, then O_2 plasma etching to selectively remove the S block, leaving behind a nanoporous AlO_x film that serves as an inorganic etching template.

5.7.3 DSA tests on various neutral mat chemistries

While multiple mats appeared to lead to similar self-assembled film quality (60S, 63S, and 67S) as described in 5.6.2, for directed self-assembly (DSA) applications this was not the case as illustrated in Figure 5.6. E-beam lithography was used to write patterns of hexagonally packed spots separated at a pitch of $2L_0$ of the PS(20k)-*b*-PMMA(50k) BCP, or 75 nm. The pattern was written at a variety of doses ranging from 30,000 μC/cm^2 to 75 μC/cm^2.

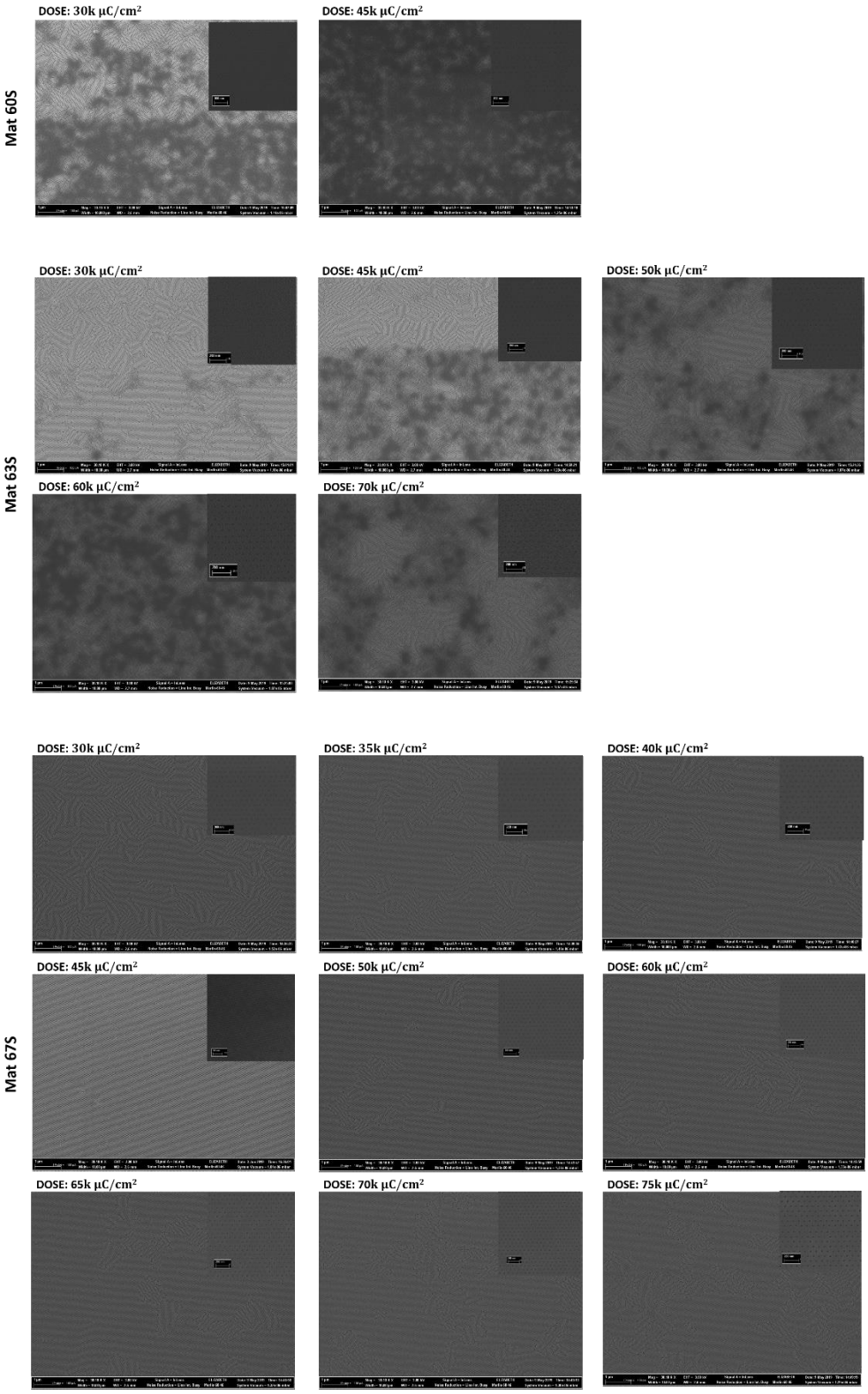


Figure 5.8 Tests conducted to assess DSA quality for 20-50 PS-PMMA on mats 6, 7, and 8 as a function of e-beam dose. Mat 8, 67S, produced the highest quality assembly in DSA application. The lowest number of defects from top-down SEM were observed for the chemical template

Figure 5.8, continued:
generated with an e-beam dose of 45k mJ/C^2. The insets show the e-beam pattern for each dose/assembly condition.

For mats 60S and 63S, significant defectivity was observed across all doses, rendering them useless for DSA (Figure 5.6). For mat 8, defectivity was low across most doses, and acceptable quality of assembly was found at a dose of 45,000 μC/cm^2, which was the dose we selected for our process. It is important to note that 67S mat resulted both in high quality DSA in the pattern area, and in high quality SA outside of the pattern area as shown in Figure 5.7. This meant that we could fabricate DSA and SA structures simultaneously on the same chip, and enable direct comparisons between the different types of structures.

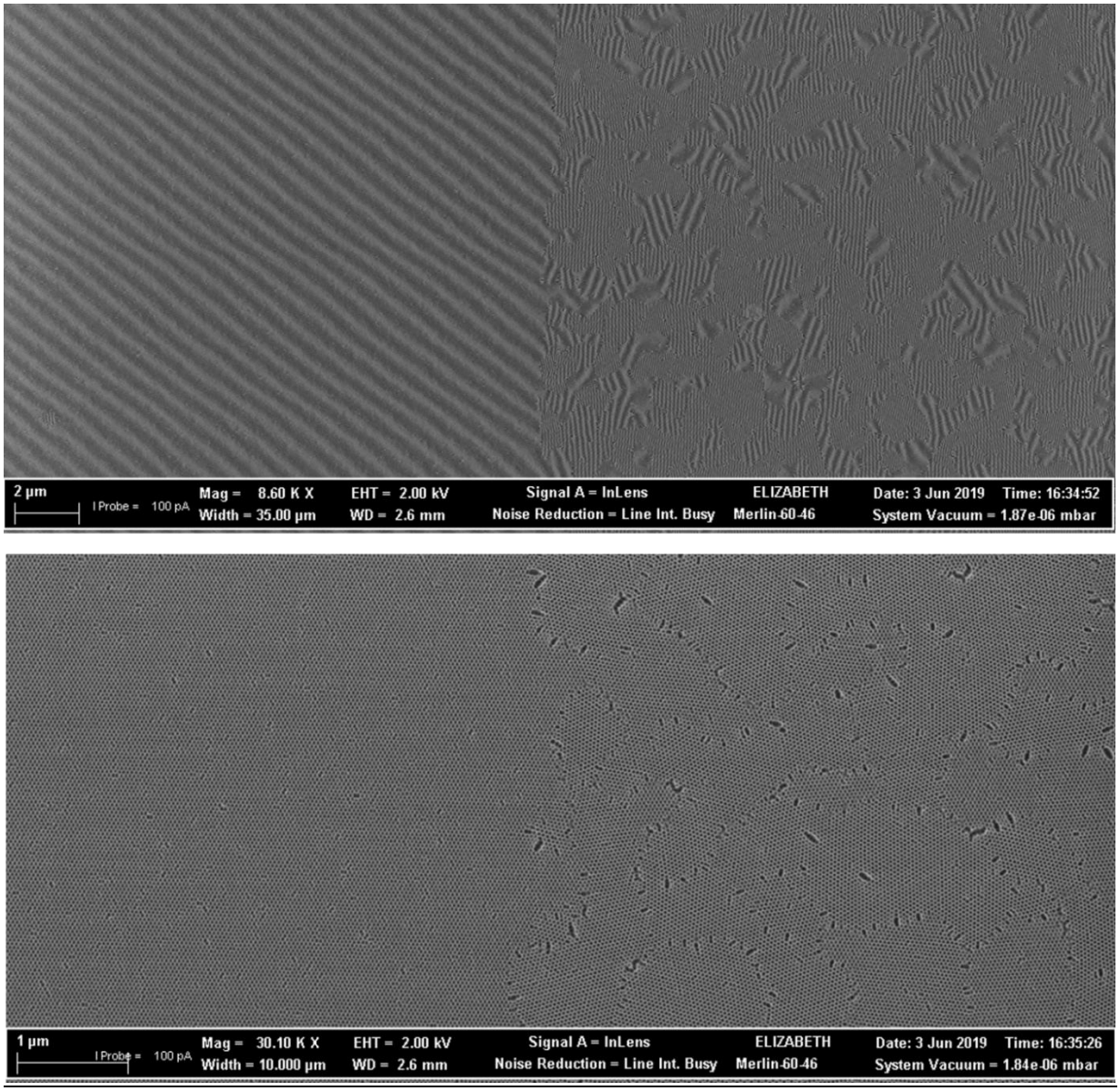


Figure 5.9 SEM micrographs showing how the assembly of the block copolymer within and outside of the chemical template. Within the pattern area, the block copolymer assembles into a large defect-free single orientation grain of hexagonal packed cylinders. Immediately outside the edges of the chemical template, the block copolymer seamlessly reverts to self-assembled morphology. In the top image, Moiré fringing can be seen illustrating the sizes of each domain with a single orientation. Heavy fringing on the right corresponds to the random orientations of self-assembled grains, while the large single orientation area on the right corresponds to the perfectly assembled BCP guided by the underlying chemical template. The bottom figure is a zoom of the top figure, showing the actual structure of the block copolymer nanostructure post-SIS.

5.7.4 Dimensional Analysis of Holes and Porosity Calculations

After full fabrication, the samples were inspected in a Carl Zeiss Merlin SEM and average porosity was calculated from the SEM micrographs at image widths of both 2 and 5μm. Some samples were not vapor-HF released and were inspected pre-etch as a reference. Due to charging effects from the underlying oxide, as well as some roughness at the edges of the pores, *P* tends to look much smaller for the pre-VHF samples vs the post-VHF samples (Figure 5.11) We consider the post-VHF released images be most accurate.

P was calculated via two softwares, Gwyddion and FIJI (Fiji is Just ImageJ). For Gwyddion analysis, an image was imported, and the SEM details bar was cropped from the bottom of the image. Next, under "Data Process", we selected "Grains", then "Mark by Threshold." We defined the threshold as masking the holes, rather than the matrix, and used the automatic thresholding of the software without adjustment. Then, under "Data Process" and "Grains", we selected "Statistics", which produces a window listing a number of parameters about the image, including relative and percent *P*. The *P* calculated by Gwyddion is the relative area of thresholded holes divided by the total area of the image.

To calculate *P* in FIJI, the image was imported, the image scale was set, and the SEM details bar was cropped out. The images were then thresholded ("Image" → "Adjust" → "Threshold") to a binary image, where the holes became black spots. The automatic thresholding in FIJI was not as good with detecting the true edge of the holes as Gwyddion, so we adjusted the threshold to completely cover the hole edge manually. Next, under "Analyze", the "Analyze Particles" tool was used to calculate a number of parameters about the holes including hole area and the centroid positions of each hole. A particle analysis tool was then used to count the thresholded pores and calculate the area of each pore.

To calculate porosity for DSA structures:

The hole areas were copied over to a MATLAB program, and the following equation was used to convert from area to calculate area to radius of each pore:

$$r = \sqrt{\frac{A}{\pi}}$$

Then, each value of *r* was used to calculate a value of *P* using the following equation:

$$P = \frac{2\pi r^2}{\sqrt{3}p^2}$$

Then, every value of P was averaged to calculate an average P for the sample. This value was compared to the P calculated using the averaged value of r, and both values were found to be similar. As all pores are created by a block copolymer with a thermodynamically defined length scale and all samples were prepared at the exact same time during the same process, defining an average *P* for all the DSA samples in our system from a few 2-3 um images is reasonable. Typically, 500-2000 pores were used to calculate these average values, depending on the magnification of the image.

Additional dimensional analysis of DSA structures:

To compute the center to center spacing, or pitch, of the DSA holes from the SEM images, we used a plugin "Nnd" to compute the distances between pairs of neighboring holes. All calculated pitches were averaged to generate an average pitch from the image. We found that our calculated pitch from this method was 3.3% smaller (1.2 nm) than the spacing of the chemical template we wrote using e-beam lithography. Since we believe the e-beam writer is better calibrated and more precise than the SEM, we calibrated all our dimensional analysis to account for this small calibration error. We found excellent agreement between our computed pitch and the

pitch defined by the spacing of our e-beam written chemical template after adjusting for SEM calibration error of 3.3%.

To compute the average neck width of our DSA structures, we used the following calculation: $neck = pitch - 2 * radius$. We calculated this value just using the average pitch and radius values, and by averaging this value across all data points, and found no difference between the two.

To calculate porosity for SA structures:

Due to the grain boundaries and associated defects in the SA structures, calculating the average *P* and other dimensions of these structures was significantly more challenging. To compute the *P* of the SA structures, a simple area fraction was calculated by dividing the area of thresholded holes over the total area of the image. We calculated this value in both Gwyddion and ImageJ and obtained good agreement. Due to the presence of grain boundaries, we did this analysis on lower resolution images that were 5 μm wide to include as many grain boundaries as possible while still having high enough magnification to ensure detail.

Additional dimensional analysis for SA structures:

We calculated the average hole area, radius, pitch, and neck widths for the non-defect, or "normal" holes in the SA structures via a more complex process than for the DSA structures. From performing dimensional analysis on the DSA structures that had no defects, we knew the size of the area, radius, and pitch distributions for a normal hole would be.

To calculate the average radius of a normal SA hole, we first calculated areas of all holes in the image via FIJI and adjusted them to account for the 3.3% calibration error of our SEM that we determined previously. Then, using the range limits of area from the DSA holes, we filtered those areas to omit all outliers below and above that range. These normal hole areas when then

used to compute the average radius for a normal hole. Similarly, the computed pitches from the image were filtered using the DSA pitch distribution as a reference, and anomalously small and large pitches were omitted. The average radius and pitch for the normal holes were used to compute the average neck width for the SA structures.

We found that the average pitch for the SA structures was slightly smaller than for the DSA structures. This is in-line with understanding of how block copolymers behave when assembling in the presence of a guiding chemical template- if the pitch of the chemical template is within a certain percentage of the native pitch, the pitch of a block copolymer structure can be defined by the chemical template, not the native pitch of the polymer. Distributions of area including both normal and defect holes were computed for SA structures to illustrate the relatively low population of outliers as shown in Figure 5.10.

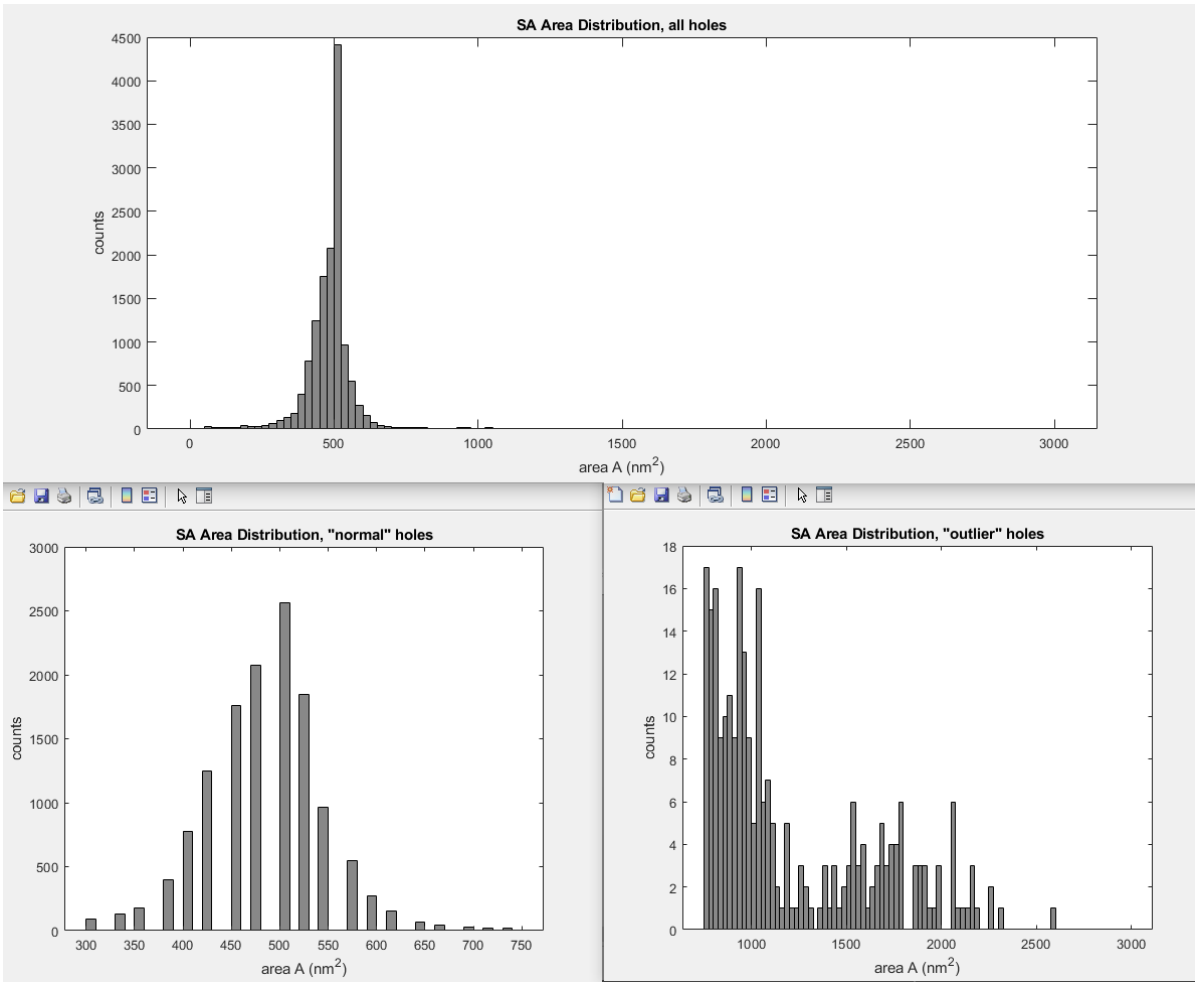


Figure 5.10 Distribution of hole areas in self-assembled structures across a 5 µm SEM micrograph. (Top) all areas are shown plotted together, including normal holes and defect outliers. (Bottom, left) the distribution of normal (non-defect) hole areas is shown. (bottom, right) the distribution of defect holes is shown. Note that the overwhelming majority of holes are normal.

5.7.5 Surface to volume ratio calculations

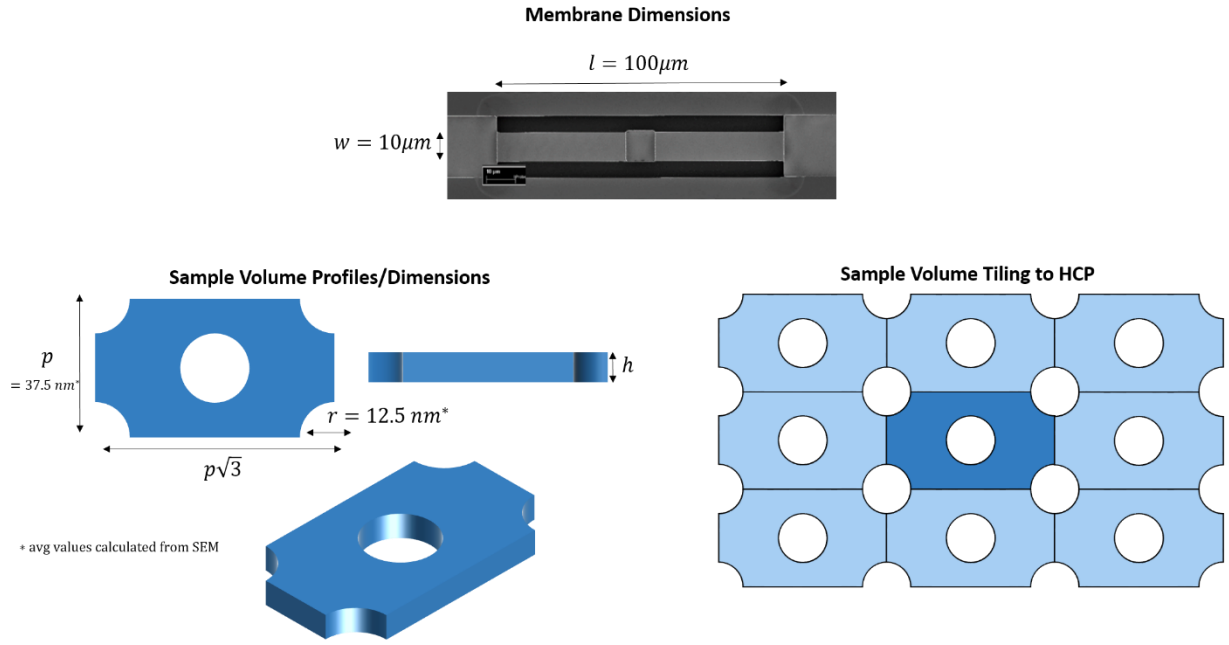


Figure 5.11 Illustrations of the unit volume used to compute s/v ratio for DSA and SA structures. The dimensions of the full membrane are shown at the top. On the bottom left, the dimensions and profile views useful for the calculation are shown. On the bottom right, the tiling of the unit volume to form the hexagonal lattice of holes is shown.

<u>For DSA structures:</u>

Assuming that the P of the top and bottom of the film were identical, area of the top and bottom surfaces for length l, width w, and P was defines as $A_{T,B} = 2lw(1 - P)$, where w and l were the overall dimensions of the suspended membrane (10 µm and 100 µm respectively).

To compute the surface area of the holes, a rectangular unit volume with two net holes was defined as illustrated in Figure 5.9**.** Using values of radius r and pitch p calculated from dimensional analysis, plus the thickness h, the surface area of the holes was computed for one unit volume, $A_{holes,unit} = 2\pi r^2 h$. This number was then multiplied by the number of unit volumes per length and width to estimate the total surface area of all holes in a membrane, $A_{holes,tot} = A_{holes,unit} * \frac{l}{p\sqrt{3}} * \frac{w}{p}$. This calculation allowed us to account for the added surface area of pores on the scalloped edges of the membranes.

To calculate the non-scalloped flat area of the sides, we multiplied the area of the flat part of the sides in the unit volume ($A_{sides,flat} = 2 * p\sqrt{3} - 2r$) by the number of unit volumes in the length of the actual membrane, $\frac{l}{A_{sides,flat}}$, to estimate the flat side area of the entire membrane. Only the long sides of the membrane were used in this calculation because the membrane is attached to the substrate at each end.

The overall surface area of the membrane was computed as: $A_{all} = A_{T,B} + A_{holes,tot} + A_{sides,flat}$. The volume of the overall membrane was calculated as $V_{all} = (1 - P)lwh$. The s/v ratio was calculated as $\text{sv} = A_{all}/V_{all}$.

For SA structures:

For SA structures, the method for estimating the s/v ratio was identical to the method used for DSA structures, with several caveats. First, we assumed that the hole-induced additional surface area at the membrane edges was the same for SA as DSA. We also assumed that the *P* at the top and bottom surfaces was the same, and that the hole profiles were vertical with a constant radius from top to bottom.

There is no straightforward way to precisely compute a s/v ratio for the entire membrane due to the random nature of grain boundaries and associated defects, and it is impossible to design a true representative unit volume. For the purposes of this calculation, we calculated an effective radius for the "average" hole size of a SA hole using the methods for FIJI radius calculation in Section 5.4, including both normal holes and oversized and undersized defect generated holes. In calculating the effective r by this approach, our calculation assumed that every hole was circular. The effective r we calculated was slightly larger than the r of the normal holes, and was how we chose to account for the presence of outlier holes for the s/v ratio calculation.

This effective r was used in place of *r* in the same calculations used to compute the s/v ratio of the DSA structures. We consider the s/v ratio calculation of our SA structures to be our best estimate, although we acknowledge that the actual value inevitably varies somewhat depending on the variability of grain boundary concentration and defect sizes endemic to SA structures.

5.7.6 Standard error calculation

Standard error for κ_{eff} was calculated via the following methodology. The relationship between τ and κ is: $\kappa = \frac{\alpha}{\tau} + \beta$. For error propagation, we used the following:

$$A = a \pm \delta a \qquad B = b \pm \delta b \qquad C \equiv A \cdot B^{-1} = \frac{a}{b}\left(1 \pm \frac{\delta a}{a} \pm \frac{\delta b}{b}\right)$$

For our calculations, $A \Rightarrow \alpha$ and $B \Rightarrow \tau \pm \Delta\tau$. The values α and β are geometry dependent and were different for the nonporous and porous membranes. For the control structures, $\alpha = 2667.6$ and $\beta = -4.5383$. For the porous structures, $\alpha = 4336.4$ and $\beta = -0.0563$.

5.7.7 Classical volume reduction effect on thermal conductivity

The classical effect of volume reduction on the thermal conductivity was calculated by FEM using the steady-state thermal analysis module in ANSYS software. Here, we first calculated the thermal conductance *G* of a thin rectangular plate with cylindrical through-holes arranged in a triangular lattice replicating our PnC films.. In this model, one of the surfaces of the nanoporous film, which we define as surface-A, was fixed at a constant temperature of T_A (= 20°C). A uniform heat flow of Q (= 2 W) was applied to surface-B. With the given κ of the Si bare film measured by TDTR, the temperature distribution of the holey film in steady state could be calculated by solving the classical heat conduction equation from Fourier's law ($\rho C_p \frac{\partial T}{\partial t} = Q + \nabla \cdot (\kappa \nabla T)$) with the ANSYS software. Using the simulated temperature of surface-B T_B, *G* of the holey film could be described as

$$G = Q/(T_B - T_A) \quad \text{(S1)}$$

The predicted thermal conductivity, $\kappa_{predicted}$, of the nanoporous Si film was calculated:

$$\kappa_{predicted} = \frac{l}{wt} G \quad \text{(S2)}$$

where w, l, and t are the width, length, and thickness of the simulated rectangular plate, respectively. The dimensions w, l, and t were fixed at 10 μm, 100 μm, and 100 nm to exactly replicate the experimental samples. We carried out the simulations for rectangular plates with a hexagonal array (pitch = 37.5 nm) of holes with fixed values of diameter (d) of 25 nm and P (ϕ) of 0.40-0.42. These simulations showed that Fourier's law, which does not include nanoscale size effects, predicts that the magnitude of $\kappa_{predicted}$ does not depend on d when the P (ϕ) of the plate is fixed. The FEM simulations also predicts that $\kappa_{predicted}$ decreases monotonically with increasing P.

5.7.8 All τ measurements for each measured device

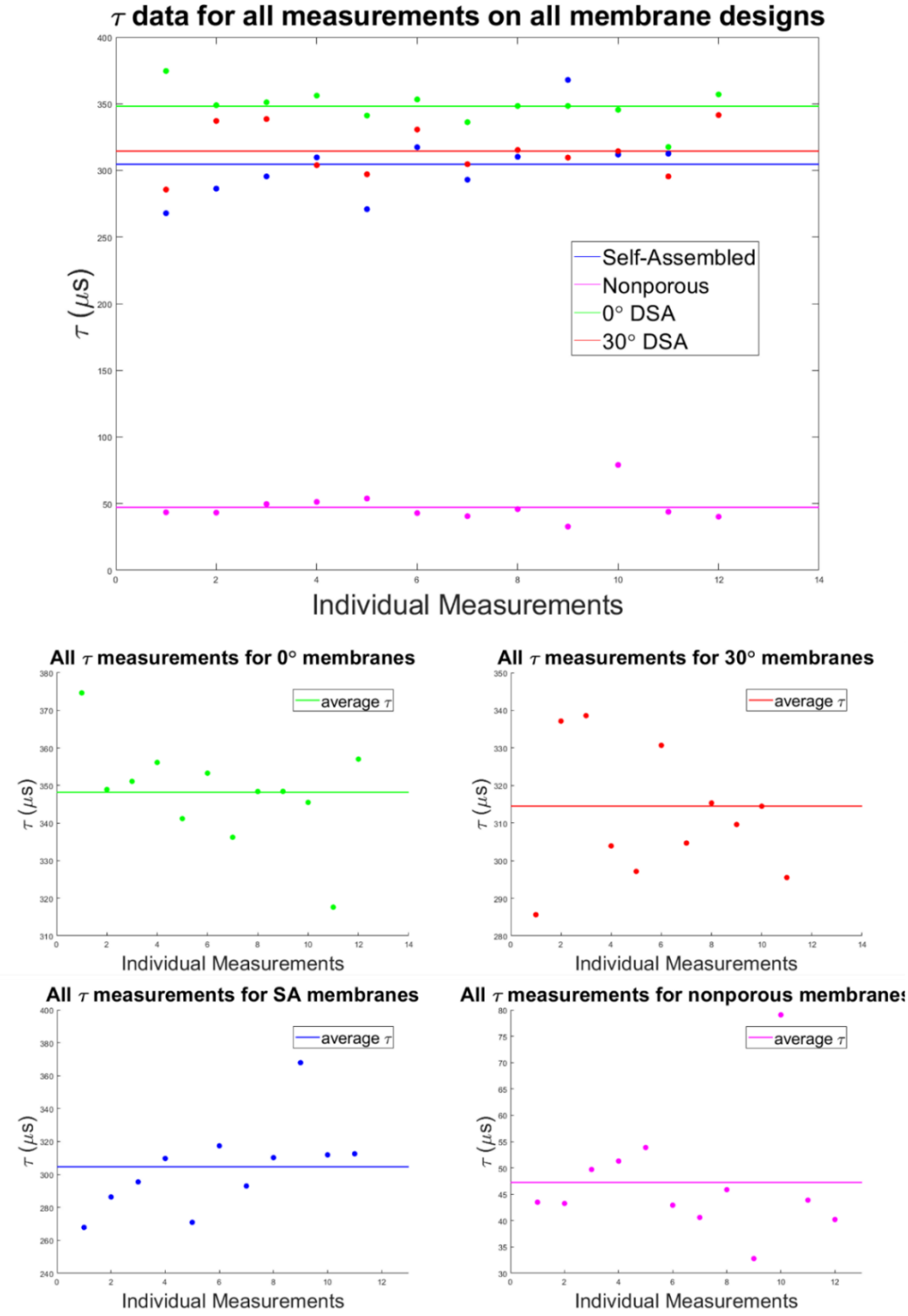


Figure 5.12 Plots of all measurements of τ. Larger τ indicates slower thermal dissipation and vice versa. To measure τ, 4 devices of each type were measured 3 times each for a total of 12 measurements per design. At the top, all 12 measurements of τ for all device designs are plotted

Figure 5.12, continued
against their average values (the solid lines). At the bottom, τ measurements for each design are plotted separately along with their average values. Note that the SA and 30° samples perform roughly equivalently as their measurements generally overlap.

5.7.9 Porosity calculations from SEM images pre- vs. post-VHF etching

We observed differences in apparent porosity when analyzing images of the nanoporous membranes both pre- and post-VHF etching as shown in Figure 5.10. In the pre-VHF images, bright halos are visible around the hole edges, causing them to appear smaller than the holes in the post-VHF images. We believe this is due to charging effects at the pore edges caused by charging effects due to the presence of the underlying oxide. We consider the post-VHF images to be more representative of the true size of the holes, as this charging effect is not present. All porosities discussed in the text are based on analysis of SEM images taken post-VHF etching.

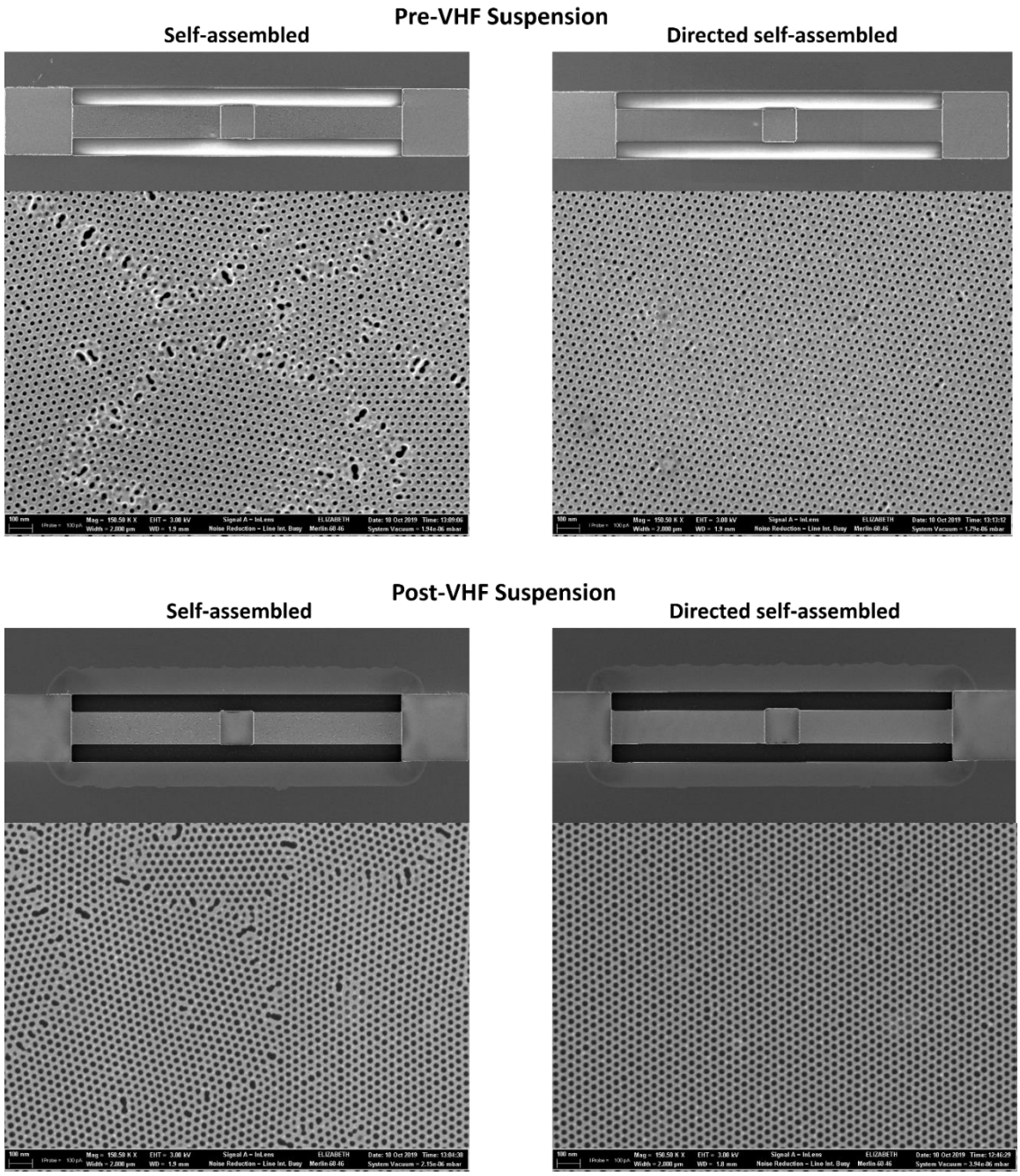


Figure 5.13: Top-down SEM micrographs of full membranes, and close-up views of the holes, pre- and post- vapor phase HF etching to suspend the membranes.

5.8 References

1. Maldovan, M. Sound and heat revolutions in phononics. (2013). doi:10.1038/nature12608

2. Stoykovich, M. P. *et al.* Directed Self-Assembly of Block Copolymers for Nanolithography: Fabrication of Isolated Features and Essential Integrated Circuit Geometries. (2007). doi:10.1021/nn700164p

3. Nomura, M., Shiomi, J., Shiga, T. & Anufriev, R. Thermal phonon engineering by tailored nanostructures. *Jpn. J. Appl. Phys.* **57**, 080101 (2018).

4. Heino, P. Dispersion and thermal resistivity in silicon nanofilms by molecular dynamics. *Eur. Phys. J. B* **60**, 171–179 (2007).

5. Hori, T. & Shiomi, J. Tuning phonon transport spectrum for better thermoelectric materials. *Science and Technology of Advanced Materials* **20**, 10–25 (2019).

6. Wang, X. & Huang, B. Computational Study of In-Plane Phonon Transport in Si Thin Films. (2014). doi:10.1038/srep06399

7. Maire, J. *et al. Heat conduction tuning using the wave nature of phonons*.

8. Yu, J.-K., Mitrovic, S., Tham, D., Varghese, J. & Heath, J. R. Reduction of thermal conductivity in phononic nanomesh structures. *Nat. Nanotechnol.* | **5**, (2010).

9. Anufriev, R., Ramiere, A., Maire, J. & Nomura, M. Heat guiding and focusing using ballistic phonon transport in phononic nanostructures. *Nat. Commun.* **8**, 1–8 (2017).

10. Verdier, M., Anufriev, R., Ramiere, A., Termentzidis, K. & Lacroix, D. Thermal conductivity of phononic membranes with aligned and staggered lattices of holes at room and low temperatures. *Phys. Rev. B* **95**, 205438 (2017).

11. Anufriev, R., Maire, J. & Nomura, M. Reduction of thermal conductivity by surface scattering of phonons in periodic silicon nanostructures. *Phys. Rev. B* **93**, 45411 (2016).

12. Takahashi, K. *et al.* Elastic inhomogeneity and anomalous thermal transport in ultrafine Si phononic crystals. *Nano Energy* **71**, 104581 (2020).

13. Zhou, C. *et al.* Cite This: ACS Nano 2020, 14, 6980−6989 ACS Nano 2020, 14, 6980−6989 Downloaded via UNIV OF CHICAGO on. (2020). doi:10.1021/acsnano.0c01463

14. Tang, J. *et al.* Holey silicon as an efficient thermoelectric material. *Nano Lett.* **10**, 4279–4283 (2010).

15. Lee, J., Lim, J. & Yang, P. Ballistic Phonon Transport in Holey Silicon. *Nano Lett* **15**, 48 (2015).

16. Cahill, D. G. Thermal conductivity measurement from 30 to 750 K: The 3ω method. *Rev. Sci. Instrum.* **61**, 802–808 (1990).

17. Sun, T., Tang, P., Qiu, F., Yang, Y. & Shi, A.-C. Formation of Single Gyroid Nanostructure by Order-Order Phase Transition Path in ABC Triblock Terpolymers. *Macromol. Theory Simulations* **26**, 1700023 (2017).

18. Nomura, M. *et al.* Impeded thermal transport in Si multiscale hierarchical architectures with phononic crystal nanostructures. *Phys. Rev. B* **91**, 205422 (2015).

19. Dechaumphai, E. & Chen, R. Thermal transport in phononic crystals: The role of zone folding effect. *J. Appl. Phys* **111**, 73508 (2012).

20. Ravichandran, N. K. & Minnich, A. J. Coherent and incoherent thermal transport in nanomeshes. *Phys. Rev. B - Condens. Matter Mater. Phys.* **89**, 205432 (2014).

21. Alaie, S. *et al.* Thermal transport in phononic crystals and the observation of coherent phonon scattering at room temperature. *Nat. Commun.* **6**, 1–8 (2015).

22. Tambo, N. *et al.* Ultimate suppression of thermal transport in amorphous silicon nitride by phononic nanostructure. *Sci. Adv.* **6**, eabc0075 (2020).

23. Maire, J., Anufriev, R. & Nomura, M. Ballistic thermal transport in silicon nanowires. *Sci. Rep.* **7**, 1–8 (2017).

24. Tang, G. H., Bi, C. & Fu, B. Thermal conduction in nano-porous silicon thin film. *J. Appl. Phys.* **114**, 184302 (2013).

25. Zhou, C. *et al.* FULL PAPER www.afm-journal.de Fabrication of Nanoporous Alumina Ultrafiltration Membrane with Tunable Pore Size Using Block Copolymer Templates. (2017). doi:10.1002/adfm.201701756

26. Tseng, Y., Peng, Q., Ocola, L. E., Elam, W. & Darling, S. B. Enhanced Block Copolymer Lithography Using Sequential Infiltration Synthesis. 17725–17729 (2011).

27. Weisbord, I., Shomrat, N., Azoulay, R., Kaushansky, A. & Segal-Peretz, T. Understanding and Controlling Polymer-Organometallic Precursor Interactions in Sequential Infiltration Synthesis. *Chem. Mater.* **32**, 4499–4508 (2020).

28. Ruiz, R. *et al.* Density multiplication and improved lithography by directed block copolymer assembly. *Science* **321**, 936–939 (2008).

29. Liu, W. & Asheghi, M. (No Title). *J. Appl. Phys* **98**, 123523 (2005).

30. He, Y., Donadio, D., Lee, J.-H., Grossman, J. C. & Galli, G. Thermal Transport in Nanoporous Silicon: Interplay between Disorder at Mesoscopic and Atomic Scales. **16**, 7 (2020).

31. Lee, J. H., Galli, G. A. & Grossman, J. C. Nanoporous Si as an efficient thermoelectric material. *Nano Lett.* **8**, 3750–3754 (2008).

32. Donadio, D. & Galli, G. Atomistic Simulations of Heat Transport in Silicon Nanowires. doi:10.1103/PhysRevLett.102.195901

33. Plimpton, S. Fast parallel algorithms for short-range molecular dynamics. *J. Comput. Phys.* **117**, 1–19 (1995).

34. Tersoff, J. Modeling solid-state chemistry: Interatomic potentials for multicomponent systems. *Phys. Rev. B* **39**, 5566–5568 (1989).

35. Hori, T., Shiomi, J. & Dames, C. Effective phonon mean free path in polycrystalline nanostructures. *Appl. Phys. Lett.* **106**, 171901 (2015).

36. Prasher, R. Transverse thermal conductivity of porous materials made from aligned nano- and microcylindrical pores. *J. Appl. Phys.* **100**, 064302 (2006).

37. Zhou, C. *et al.* Combining double patterning with self-assembled block copolymer lamellae to fabricate 10.5 nm full-pitch line/space patterns. *Nanotechnology* **30**, 455302 (2019).

38. Hur, S.-M., Thapar, V., Ramírez-Hernándezhernández, A., Nealey, P. F. & De Pablo, J. J. Defect Annihilation Pathways in Directed Assembly of Lamellar Block Copolymer Thin Films. (2018). doi:10.1021/acsnano.8b04202

39. Lim, J. *et al.* Simultaneous thermoelectric property measurement and incoherent phonon transport in holey silicon. *ACS Nano* **10**, 124–132 (2016).

40. Honarvar, H. & Hussein, M. I. Two orders of magnitude reduction in silicon membrane thermal conductivity by resonance hybridizations. *Phys. Rev. B* **97**, 195413 (2018).

41. Jeng, M. S., Yang, R., Song, D. & Chen, G. Modeling the thermal conductivity and phonon transport in nanoparticle composites using Monte Carlo simulation. in *Journal of Heat Transfer* **130**, (American Society of Mechanical Engineers(ASME), 2008).

42. Verdier, M., Termentzidis, K. & Lacroix, D. Crystalline-amorphous silicon nano-composites: Nano-pores and nano-inclusions impact on the thermal conductivity. *J. Appl. Phys.* **119**, 175104 (2016).

43. Ju, Y. S. & Goodson, K. E. Cite as. *Appl. Phys. Lett* **74**, 3005 (1999).

44. Hopkins, P. E. *et al.* Reduction in the thermal conductivity of single crystalline silicon by phononic crystal patterning. *Nano Lett.* **11**, 107–112 (2011).

45. Tian, Y., Puurtinen, T. A., Geng, Z. & Maasilta, I. J. Minimizing Coherent Thermal Conductance by Controlling the Periodicity of Two-Dimensional Phononic Crystals. *Phys. Rev. Appl.* **10**, 14008 (2019).

46. Zen, N., Puurtinen, T. A., Isotalo, T. J., Chaudhuri, S. & Maasilta, I. J. Engineering thermal conductance using a two-dimensional phononic crystal. *Nat. Commun.* **5**, 3435 (2014).

47. Prasher, R., Tong, T. & Majumdar, A. Approximate analytical models for phonon specific heat and ballistic thermal conductance of nanowires. *Nano Lett.* **8**, 99–103 (2008).

48. Dames, C. & Chen, G. Theoretical phonon thermal conductivity of Si/Ge superlattice nanowires. *J. Appl. Phys.* **95**, 682–693 (2004).

49. Tang, J. *et al.* Holey silicon as an efficient thermoelectric material. *Nano Lett.* **10**, 4279–4283 (2010).