Dual relaxation oscillations in a Josephson-junction array

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We report relaxation oscillations in a one-dimensional array of Josephson junctions, wherein the array dynamically switches between low-current and high-current states. The oscillations are current-voltage dual to those ordinarily observed in single junctions. The current-voltage dual circuit quantitatively accounts for temporal dynamics of the array, including the dependence on biasing conditions. Injection locking of the oscillations results in well-developed current plateaux. A thermal model explains the self-consistent reduction of the superconducting gap due to overheating of the array in the high-current state. Our work suggests that overheating determines the switching from the high-current state to the low-current state.

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I. INTRODUCTION

A current-biased Josephson junction is hysteretic in measured voltage. When voltage biased, such a junction can undergo ordinary relaxation oscillations controlled by an inductive time constant, generating voltage plateaux when phase locked [1,2]. In the electrically dual scenario, of interest here, a voltage-biased device exhibits hysteretic behavior in measured current [Fig. 1(a)]. When current biased, it undergoes dual relaxation oscillations controlled by a capacitive time constant, generating current plateaux when phase locked.

Here, we observe relaxation oscillations in a current-biased one-dimensional array of Josephson junctions. These oscillations are described by a circuit model, current-voltage dual to the ordinary Josephson relaxation oscillations [1]. Injection locking of the dual relaxation oscillations results in current plateaux. The high-current state is found to obey a characteristic self-consistent relation, suggesting that it is governed by overheating effects.

Our platform for studying dual relaxation oscillations is a chain of 1217 Al/AlO_x Josephson junctions fabricated by a standard Dolan bridge process using electron-beam lithography [Fig. 1(b)]. Measurements are performed with the use of standard transport techniques, with filtering and methods described in Ref. [3] and Appendix E. An external current source imposes an average current $\langle I \rangle$. Instantaneous current $I(t)$ through the device is measured with a commercial transimpedance amplifier, and instantaneous voltage drop $V(t)$ is measured with a differential voltage amplifier. The set cryostat temperature is 8 mK unless otherwise stated. The arrays we study are known to exhibit weak supercurrent features visible at low bias [3]. At large bias these features are not apparent, and the system exhibits a resistive low-bias branch with a hysteretic critical voltage and a hysteretic relaxation voltage (Appendix A). Above the critical voltage, all the junctions in the array are turned normal, and the array exhibits Ohmic behavior, leading to Joule overheating, which in turn reduces the superconducting gap. The transition from high to low current occurs when the bias voltage across each junction approximately equals twice the reduced superconducting gap. Similar voltage hysteresis has been observed in the very different regime of fully insulating arrays [4–6]. The hysteretic I-V characteristic of the chain gives rise to relaxation oscillations in certain ranges of bias currents.

Relaxation oscillations emerge when an external current bias $\langle I \rangle$ is imposed in the unstable regime. The oscillations are characterized by a periodic, spiking voltage signal, reminiscent of a charge-discharge cycle of a capacitor [Fig. 1(d)]. We have verified that changing room-temperature biasing circuitry does not qualitatively alter the oscillations. Parametrically plotting the instantaneous measured current and voltage reveals a relaxation orbit with distinct low-current and high-current regions [Fig. 1(c)]. Correlating low-current and high-current states to the time-domain voltage oscillations, one can seen that in the low-current state the voltage steadily increases, until the system quickly transitions to the high-current

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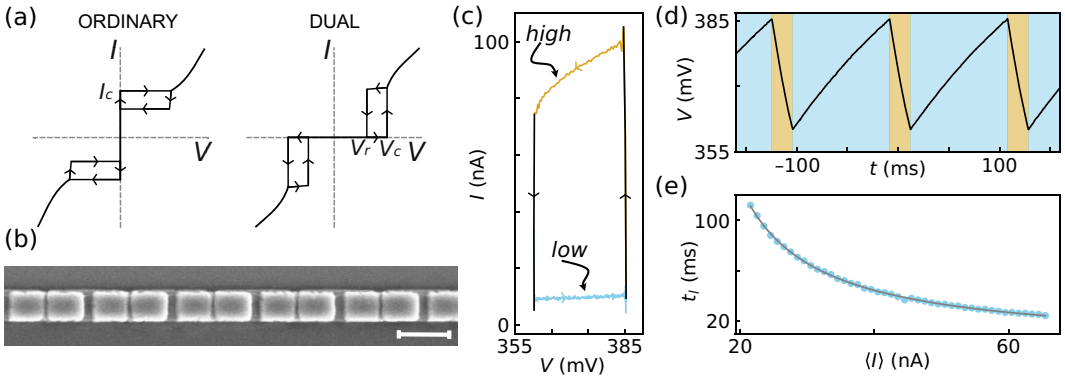

FIG. 1. Phenomenology of dual relaxation oscillations. (a) Schematic-voltage characteristic of a current-biased Josephson-junction array (left) and a voltage-biased Josephson-junction array (right). Arrows indicate orbits of relaxation oscillations for the ordinary (left) and dual (right) cases. Note that the ordinary and dual case have opposite chirality orbits. I_c is the critical current. V_g is the superconducting gap voltage. V_r is the relaxation voltage. V_c is the critical voltage. (b) Scanning electron micrograph of the device studied. The scale bar represents 1 μm. (c) Parametric plot of the measured current $I(t)$ versus the measured voltage $V(t)$ in the presence of a current bias $\langle I\rangle$, consistent with the hysteretic behavior illustrated on the right in (a). Regions of low current and high current are indicated. Four arrowheads are added to illustrate chirality of the current-voltage orbit. (d) Voltage V measured as a function of time t. The blue regions represent low-current states and the orange regions represent high-current states [as illustrated in (c)]. The plots in (c),(d) are obtained when the array is biased with a current $\langle I\rangle = 23.5$ nA. (e) Extracted dwell time t_l (in the low-current state) as function of the biasing current $\langle I\rangle$. The gray curve represents a fit to Eq. (3). The bias current is denoted as $\langle I\rangle$ because it fixes the time-averaged current flowing in the circuit.

state, where the voltage steadily decreases. On the basis of the chirality of the current-voltage orbit, the observed relaxations are unambiguously of the dual type.

The time spent in each state depends on the external biasing conditions. Plotting the low-current state dwell time t_l at different bias currents $\langle I\rangle$ shows that t_l smoothly decreases as $\langle I\rangle$ is increased [Fig. 1(e)]. We have checked that the complementary dwell time t_h in the high-current state has the opposite dependence on bias (Appendix C), and that the time average of the instantaneous current over a cycle corresponds to the externally applied bias.

II. PROPOSED CIRCUIT MODEL

For a quantitative understanding of the dual relaxation oscillations, we introduce an effective circuit model consisting of a parallel RC circuit fed by a current source $\langle I\rangle$ [Fig. 2(b)]. Our model is the current-voltage dual to the circuit for regular Josephson relaxation oscillations [1]; see Fig. 2(a) and Appendix D. The circuit has two states, corresponding to the low-current and high-current oscillation states, controlled by a switch.

In the low-current state the Josephson-junction array is represented by a resistance $R_{\rm QP}$, and the total circuit resistance $R_{||}$ is the parallel of the device resistance and the current-source output impedance R_s, $R_{||} = (R_s^{-1} + R_{\rm QP}^{-1})^{-1}$. The device voltage V approaches the steady-state $\langle I\rangle R_{||}$ with time constant $\tau_l = R_{||}C$, according to

$$V(t) = V_r + \left(\langle I\rangle R_{||} - V_r\right)\left(1 - \exp(-t/\tau_l)\right). \quad (1)$$

However, V does not reach its steady-state value. Rather, when $V = V_c$, the switch flips to the high-current state, where the array acts as a current source I_a. The output voltage then approaches the steady-state value $(\langle I\rangle - I_a)R_s$ with time constant $\tau_h = R_sC$, according to

$$V(t) = V_c + \left(\left(\langle I\rangle - I_a\right)R_s - V_c\right)\left(1 - \exp(-t/\tau_h)\right). \quad (2)$$

When $V = V_r$, the switch flips back to the low-current state, and the cycle repeats.

The dynamics can be solved for the dwell time in each state. The dwell time in the low-current state is

$$t_l = \tau_l \ln\left(1 + \frac{V_r - V_c}{V_c - \langle I\rangle R_{||}}\right), \quad (3)$$

and the dwell time in the high-current state is

$$t_h = \tau_h \ln\left(1 + \frac{V_c - V_r}{V_r - (\langle I\rangle - I_a)R_s}\right). \quad (4)$$

For comparison with experiment, V_c and V_r are fixed by our identifying the switching voltages in Fig. 1(d). $R_{\rm QP} = 44.4$ MΩ is fixed from a linear fit to wide bias current-voltage data (Appendix A), which we speculate may be substantially affected by overheating even in the low-current state. The dwell time data in Fig. 1(e) are then fit to Eq. (3), yielding $R_s = 460$ MΩ and C. The fit capacitance $C = 53.2$ nF is close to the value from filters in the measurement setup (47 nF) [3]. The remaining free parameter, I_a, is found by our fitting t_h versus $\langle I\rangle$ to Eq. (4) with

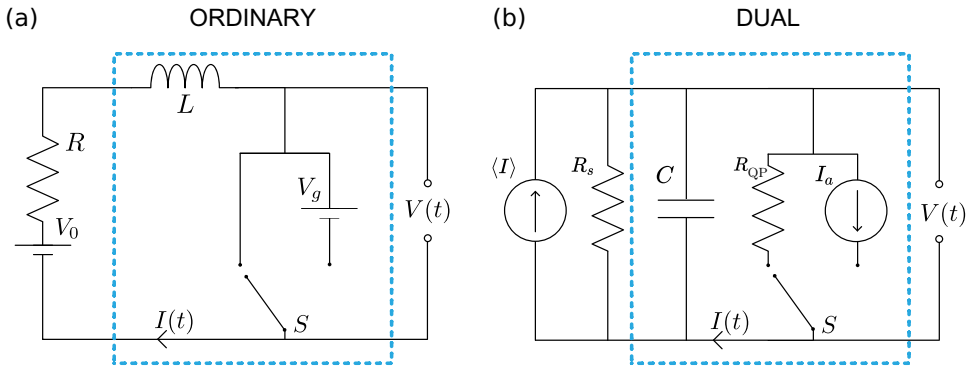

FIG. 2. Ordinary and dual circuit models. (a) Simplified circuit model for ordinary Josephson relaxation oscillations, as described in Ref. [1]. The dashed blue box represents the cryostat. V_0 is the applied voltage bias, R is the net resistance, and L is the net inductance of the circuit. The switch S changes the circuit between the supercurrent state at $V = 0$, when the junction behaves as a short circuit, and the quasiparticle-current state at $V = V_g$, when the junction behaves as a battery. (b) The dual circuit in the case of a Josephson-junction array. $\langle I \rangle$ is the applied current bias, R_s denotes the output impedance of the current biasing unit, and C denotes the net capacitance associated with the circuit. The switch S changes the circuit between the low-current state and the high-current state. In the low-current state l [blue section of the I-V characteristic in Fig. 1(c)], the array is in its quasiparticle branch with resistance $R_{\rm QP}$. In the high-current state [orange section of the I-V characteristic in Fig. 1(c)], the array is approximated as a constant current source I_a, following Ref. [1]. In reality, the array has a finite resistance, which we speculate could also be added to the model to include accuracy (see Appendix B). $V(t)$ indicates the measured voltage and $I(t)$ indicates the measured current.

all other parameters held fixed (Appendix C). The fit value $I_a = 87.2$ nA is compatible with typically observed current values in the high-current state (approximately 90 nA).

It is interesting to note that in Fig. 1(d) the voltage changes faster in the high-current state than in the low-current state even though $\tau_h > \tau_l$. The reason is that, at the biasing conditions chosen, the decay amplitude in the high-current state, $-A_h = (\langle I \rangle - I_a)R_s - V_c \approx -30$ V, is much larger than the decay amplitude in the high-current state, $A_l = \langle I \rangle R_{||} - V_r \approx 0.6$ V. The typical rate of voltage change A_l/τ_l, A_h/τ_h is then greater in the high-current state, $A_h/\tau_h > A_l/\tau_l$, for the biasing parameters in Fig. 1(d).

III. COMPARISON OF EXPERIMENTAL OBSERVATIONS AND CURRENT-VOLTAGE DUAL CIRCUIT MODEL

Having fixed all parameters within the dual relaxation model, we can now directly compare it with the full behavior of dual relaxation oscillations. Our measuring the time-resolved voltage oscillations at different current biases reveals the oscillation time period to be shorter at intermediate biases (30 nA $> \langle I \rangle >$ 60 nA) than at extremal biases [Fig. 3(a)]. The measured current shows a similar behavior [Fig. 3(b)], with distinct regions of low current and high current [see Fig. 7(b) in Appendix B]. Voltage and current calculated from the dual relaxation circuit, within the bias range 21.5 nA $< \langle I \rangle <$ 65.5 nA, have excellent qualitative agreement with the experimental observations [Figs. 3(c) and 3(d)]. This provides strong evidence that our oscillations are circuit-dual to the ordinary Josephson relaxation oscillations.

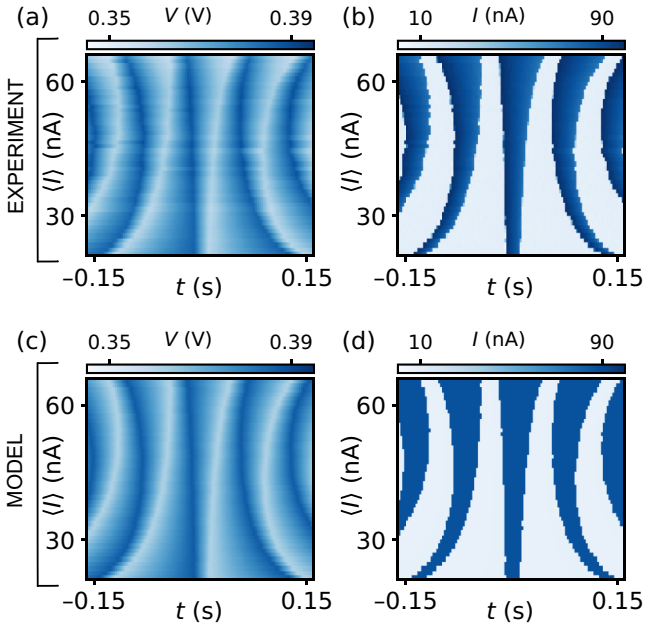

FIG. 3. Dual relaxation oscillations. Measured relaxation oscillations of (a) the voltage V and (b) the current I as a function of time t and bias current $\langle I \rangle$. Predicted (c) $V(t, \langle I \rangle)$ and (d) $I(t, \langle I \rangle)$. Voltage is calculated from Eqs. (1) and (2). Current in the low-current state is calculated from $V(t)/R_{\rm QP}$, with our taking $V(t)$ from Eq. (1). Current in the high-current state is simply I_a. In (c),(d), $t = 0$ is fixed independently for each bias current by comparison with the corresponding experimental traces, causing a slight timing jitter.

IV. PHASE-LOCKED OSCILLATIONS

To gain further insight into the temporal dynamics of the oscillations, we inject a sinusoidal locking signal with amplitude and frequencies comparable to the voltage oscillations and measure the average voltage over an integer number of time periods. In contrast to the unlocked state, where the dual relaxation oscillations appear to generate noise [Fig. 4(a)], in the presence of the locking excitation a series of well-developed current plateaux emerge [Fig. 4(b)]. Doubling the locking frequency approximately halves the number of observed current plateaux [Fig. 4(c)]. Measuring the phase-locked average voltage versus current traces for a range of locking frequencies results in a fan of current plateaux in the current-frequency plane [Fig. 4(d)].

The I-V characteristics in the locked state are also quantitatively different from the I-V characteristics in the unlocked state. The amplitude of current plateaux in the locked state is approximately 5 mV, which is several times smaller than the voltage noise amplitude in the unlocked state of approximately 20 mV [Figs. 4(a)–4(c)]. In addition, the voltage measured in the locked state is shifted by approximately 25 mV when compared with the unlocked state. It is also interesting to note that the current steps are observed only for high bias currents $\langle I\rangle \gtrsim 55$ nA.

A detailed understanding of the phase-locked oscillations is beyond our reach. However, they are qualitatively compatible with expectations based on current-voltage duality. For ordinary Josephson relaxation oscillations, phase locking is known to generate voltage plateaux [1]. We have observed the electrically dual relaxation oscillations, and the corresponding electrically dual current plateaux. Up to this point our analysis has been at a circuit level, phenomenologically encoding dynamics at V_c and V_r with a switching circuit element. This analysis is sufficient for demonstrating that we have observed a current-voltage dual to ordinary Josephson relaxation oscillations, but leaves open the underlying cause. Below we argue that thermal effects play an important role in the switching physics.

V. THERMAL MODEL

To gain insight into the microscopic mechanism governing the relaxation physics, we have measured the relaxation voltage $V_r(B,T)$ in a stable, voltage-biased configuration as a function of the in-plane magnetic field B and cryostat temperature T. V_r is insensitive to small temperature changes, but decreases dramatically in the vicinity of aluminum's critical superconducting temperature $T_{c,0} \approx 1.2$ K [Fig. 5(a)], confirming the superconducting origin of the relaxation oscillations. The applied magnetic field decreases V_r and moves its temperature dependence down to lower scales.

A simple picture of overheating, along the lines suggested in Ref. [4], explains the evolution of $V_r(B,T)$. The fundamental assumption, motivated by the picture of quasiparticle tunneling through a series of superconductor-insulator-superconductor junctions, is that the array switches at a voltage proportional to the superconducting

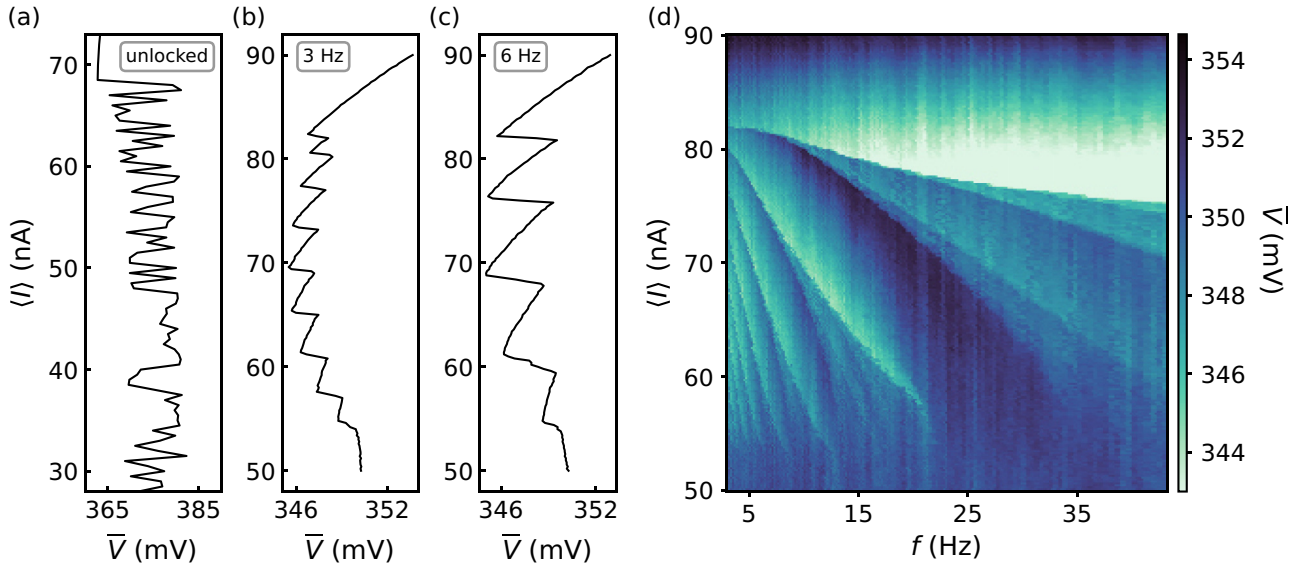

FIG. 4. Current steps in voltage-locked traces. (a) Bias current $\langle I\rangle$ as a function of measured voltage $\overline{V}$. $\overline{V}$ represents the voltage recorded after averaging over a few cycles of V versus t data. (b) Current bias as a function of measured voltage with a locking frequency of 3 Hz. (c) Same measurement as in (b) with a locking frequency of 6 Hz. To increase the signal-to-noise ratio, data in (b),(c) are plotted after averaging over 50 measurement runs. (d) Voltage $\overline{V}$ measured as a function of bias current $\langle I\rangle$ and locking frequency f .

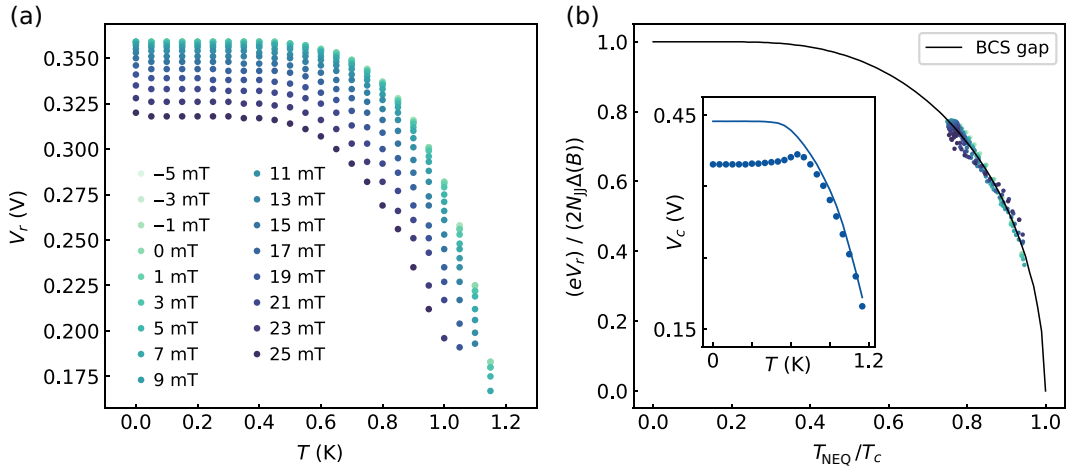

FIG. 5. Role of heating in generating hysteresis. (a) Relaxation voltage V_r as a function of temperature T at various magnetic fields. The magnetic field is applied in the plane of the chip, perpendicular to the axis of the Josephson-junction chain. (b) Plotting of the normalized V_r against the normalized, nonequilibrium effective temperature (T_{NEQ}/T_c) collapses the data in (a); see Eq. (5). The solid black line represents the normalized BCS gap function. The inset shows the temperature dependence of the critical voltage V_c. The solid blue line represents the expected equilibrium evolution $eV_c = 2N_{\mathrm{JJ}}\Delta(T)$.

gap. Note that, by construction, in this model switching is not explicitly dependent on the Josephson energy, and is not dependent on Fraunhofer corrections to the Josephson energy. In the high-current state, Joule heating reduces the superconducting gap, resulting in $V_r < V_c$. We make a few simplifying assumptions to arrive at a tractable model. Relaxation is assumed to occur when each junction is biased by twice the superconducting gap Δ, $eV_r = 2N_{\mathrm{JJ}}\Delta(B, T_{\mathrm{NEQ}})$. The gap is assumed to be spatially uniform, but to depend on a single nonequilibrium effective temperature T_{NEQ}, found from the condition that Joule heating balances cooling due to electron-phonon coupling, $I_r V_r = \Sigma\mathcal{V}(T_{\mathrm{NEQ}}^5 - T^5)$, where I_r is the current at the relaxation point, Σ is the electron-phonon coupling, $\mathcal{V}$ is the device volume, and T is the cryostat temperature. At nonzero magnetic fields, the gap is approximated as retaining a BCS form Δ_{BCS} [7], and as being scaled from its zero-field value according to $\Delta(B,T) = \Delta(B)\Delta_{\mathrm{BCS}}(T/T_c)/\Delta_0$, where $\Delta(B) = \Delta_0\sqrt{1-(B/B_c)^2}$, and $T_c = T_{c,0}\sqrt{1-(B/B_c)^2}/\sqrt{1+(B/B_c)^2}$ based on a two-fluid model with weak quadratic pair breaking [8]. Here Δ_0 is the zero-temperature, zero-field gap and B_c is the critical field. Combining the expression for $\Delta(B)$ with the criteria for relaxation, we obtain

$$\frac{eV_r}{2N_{\mathrm{JJ}}\Delta(B)} = \frac{\Delta_{\mathrm{BCS}}(T_{\mathrm{NEQ}}/T_c)}{\Delta_0}. \tag{5}$$

Given measured I_r and V_r, Eq. (5) constitutes a self-consistency test for thermal relaxations. If obeyed, the scaled relaxation voltage (left-hand side) is equal to the normalized BCS gap function at a self-consistent, nonequilibrium temperature T_{NEQ} (right-hand side).

Equation (5) is fit to the experimentally measured I_r and V_r with Σ, B_c, and $T_{c,0}$ as free parameters. Our scaling the data with the best-fit parameters results in a reasonable collapse of the data onto the normalized BCS gap function, as expected [Fig. 5(b)]. The best-fit parameter values agree with physical expectations: $T_{c,0} = 1.26$ K and $\Sigma = 0.5$ nW/μm^3 K^5 are typical of aluminum [4,9,10], and $B_c = 68$ mT is compatible with the expected critical field of the thicker islands in our chain [3]. Both the collapse of the data and the agreement of fit parameters with expectations suggest that the high-current state is dominated by thermal effects.

The critical voltage V_c is not described by a thermal model. In the low-temperature limit, V_c is 20% smaller than expected [Fig. 5(b), inset], which could perhaps be explained by overheating even in the low-current state. Overheating in the low-current state could also explain the small value of R_{QP}. Curiously, however, V_c increases slightly as temperature is increased, which disagrees with the expected dependence for equilibrium switching, and cannot be explained by overheating alone. Near the aluminum critical temperature, behavior consistent with the thermal model is recovered for V_c.

VI. SUMMARY AND OUTLOOK

We have uncovered thermal effects in the superconducting state of a one-dimensional Josephson-junction array. Our thermal model sheds light on the origin of hysteresis in voltage-biased arrays; the nonequilibrium effective temperature T_{NEQ} resulting from Joule heating scales the superconducting gap such that the chain relaxes to a low-current state at a voltage V_r lower than the critical voltage

V_c. On the basis of our analysis, Joule overheating results in $T_{\mathrm{NEQ}} \approx 0.9$ K at base cryostat temperature.

Our proposed dual relaxation circuit model explains the temporal relaxation dynamics of a current-biased Josephson-junction array. Phase locking to the voltage oscillations produces current plateaux, which are current-voltage dual to the voltage plateaux observed in ordinary Josephson relaxation oscillations [1].

We have not determined strict requirements for observing the dual relaxation oscillations. Qualitatively, it is likely important to have both a sufficiently long Josephson-junction array and a sufficiently large filter capacitance. Long arrays are required to generate Joule heating, which in turn leads to the presence of a long-lived high-current state. Large filter capacitance not only lengthens the timescale for the oscillation but more fundamentally provides the energy required for the system to switch between the low-current state and the high-current state. Based on the current-voltage duality between our circuit and that of Ref. [1], we expect that the criterion for "instantaneous switching" assumed in our model translates into $CV_c^2 \gg LI_a^2$, where L is the array inductance. In terms of the more physical normal-state device resistance $R_N \approx V_c/I_a$, this criterion becomes $R_N \gg \sqrt{L/C}$. We hope that our work inspires the criteria for dual relaxation oscillations to be further investigated in other device geometries.

Overall, our work emphasizes thermal load management in the superconducting state of a Josephson-junction chain. In contrast to our earlier work studying thermal effects in equilibrium [3], this work studies overheating at large applied bias.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this article are openly available [11], embargo periods may apply.

APPENDIX A: WIDE BIAS *I-V* CHARACTERISTICS

In the main text, we discussed the voltage oscillations resulting from the bistability in a current-biased device. Figure 6 shows the voltage-biased curves and the region of bistability (between V_r and V_c), resulting from voltage up-sweep and down-sweep on the same device. Note that the bistable region for positive voltage biases is the same as the one described in Fig. 1(c). This serves as a consistency check between the voltage-biased and current-biased curves.

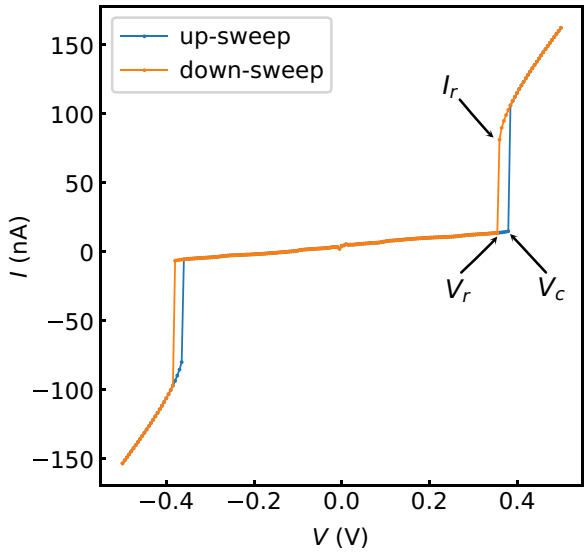

FIG. 6. Current-voltage characteristics of the Josephson-junction chain. V_c is the critical voltage, V_r is the relaxation voltage, and I_r is the current at the relaxation point.

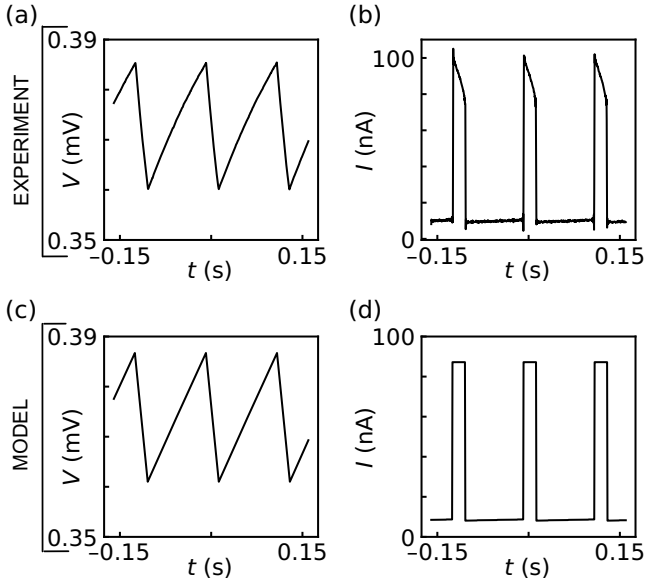

FIG. 7. Cuts at $\langle I \rangle = 23.5$ nA from Fig. 3. (a) Relaxation oscillations of the voltage V measured as a function of time t. (b) Measured current I versus time t corresponding to the region of relaxation oscillations. The periods of low current t_l and high current t_h are clearly distinguishable. (c) Calculated voltage V versus time t obtained with Eqs. (1) and (2), based on the circuit model in Fig. 2(b). (d) Calculated current I versus time t within the theoretical model.

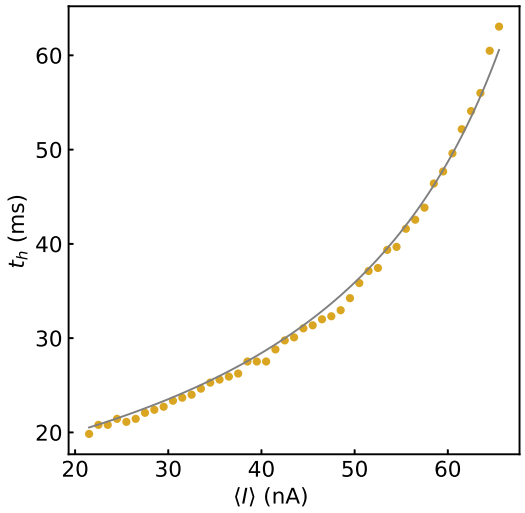

FIG. 8. Extracted dwell time t_h as a function of biasing current $\langle I \rangle$. The gray curve represents a single-parameter fit to Eq. (4) for I_a.

APPENDIX B: TEMPORAL RESPONSE PREDICTED FROM THE MODEL

In Sec. III, we compare plots from experiment and the model over two-dimensional parameter space. In Fig. 7, we explicitly compare the voltage and current, versus time, by taking cuts from the data in Fig. 3. The calculated current in Fig. 7(d) is constant in the high-current state, which is expected from the model due to the absence of any output impedance in the current generator I_a. Physically, this results from our ignoring the finite resistance of the array in the high-bias regime.

APPENDIX C: FIT OF HIGH-CURRENT STATE DWELL TIMES

We mentioned earlier that the circuit parameters in the proposed model are derived from the fitting of Eqs. (3) and (4) to the dwell time data. Figure 8 shows a plot of high-current state dwell times versus biasing current, complementing the plot in Fig. 1(e). At higher bias currents $\langle I \rangle$, the system ends up spending most of its time in the high-current state, as evident from the asymmetry in the hysteretic region in Fig. 6. Hence, the dwell time in the high-current state increases with higher bias current, while the dwell time in the low-current stat decreases [Fig. 1(e)].

APPENDIX D: CURRENT-VOLTAGE DUALITY WITH JOSEPHSON RELAXATION OSCILLATIONS

It is interesting to note that the expressions for t_l and t_h [Eqs. (3) and (4)] are analogous to the expressions worked out for ordinary Josephson relaxation oscillations [1], albeit with $V_r = 0$. The current-voltage duality

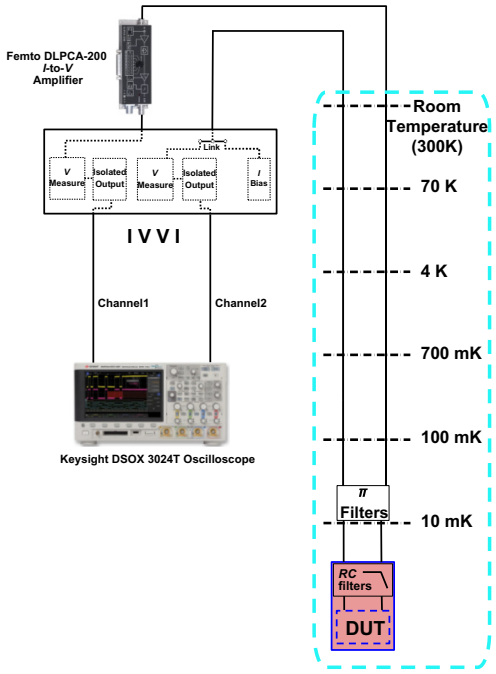

FIG. 9. Experimental setup for measuring voltage and current oscillations. The dilution fridge is represented as a dashed cyan box. Separate channels are used for current and voltage measurements on the oscilloscope. DUT, device under test.

substitutions are $I_c R \to V_c$ and $V_g \to I_a R_s$. Depending on the state (high current or low current), $L/R \to R_s C$ or $R_{||} C$, and $V_0 \to \langle I \rangle R_s$ or $\langle I \rangle R_{||}$.

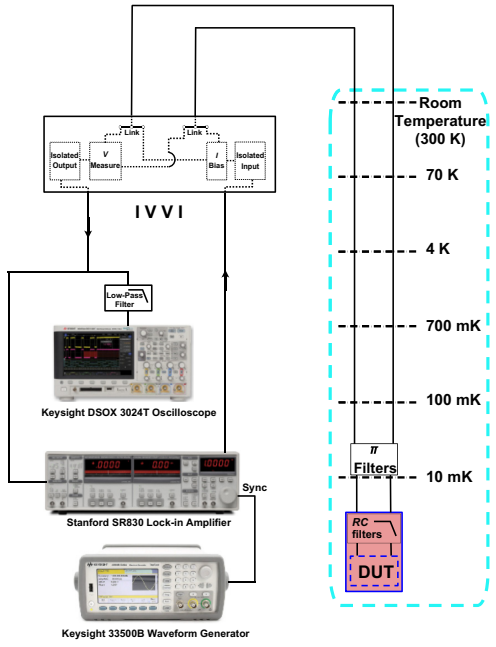

FIG. 10. Experimental setup for measuring locked-voltage oscillations. The dilution fridge is represented as a dashed cyan box. The waveform generator was used to generate a sinusoidal signal, to which the lock-in was synced. DUT, device under test.

APPENDIX E: EXPERIMENTAL SETUPS

The voltage oscillations in the current-biased Josephson-junction array were measured when the device was bonded in a two probe configuration. Hence, "link" provided on the IVVI rack was used for simultaneous measurement of current and voltage, as shown in Figs. 9 and 10. A detailed description of the device and the experimental setup is provided in Ref. [3].

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